Vectrawave
RF & Millimeter Wave MMIC Design

DC to 27GHz
Low Noise Amplifier

VM015D

General Description

The VM015D is a wide band distributed amplifier designed on a 150nm pHEMT process that operates up to 31GHz, with flat group delay.

The device is capable of more than 18dBm saturated output power, and provides more than 13dB of gain from DC to 27GHz with less than 1dB of flatness. It integrates an output power detector for monitoring function.

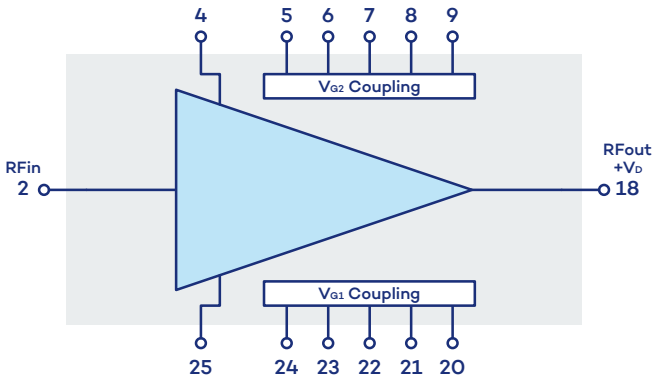
Features

Distributed amplifier pHEMT GaAs MMIC	
Wide band	**DC – 27GHz @ 1dB flatness** **DC – 31GHz @ 3dB cut_off**
Bessel response up to 40GHz with flat group delay	
50ΩRF Single ended RF input and output, DC coupled	
High P1dB	**>+15dBm DC to 27GHz**
P_{SAT}	**>+18dBm**
Small signal gain	**13dB from DC to 27GHz**
Power supply	**125mA @ +8V**
Chip size	**2.97 x 1.52 x 0.1 (mm)**

Applications

- Wide Band Low Noise Amplifier
- Radar / ECM / ECCM
- Broadband radio communication
- Optical communication: NRZ 10, 28 to 32GBps
- NRZ Nyquist Filtered 56GBps

Pins Assignement & Functional Block Diagram



Function	Pin number
RF in	2
V_{G2}	4
V_{G2} Coupling	5 / 6 / 7 / 8 / 9
RF out & V_D	18
V_{G1} Coupling	20 / 21 / 22 / 23 / 24
V_{G1}	25
Gnd	1 / 3 / 17 / 19

Electrical Specifications

Test conditions: unless otherwise noted
- T_{amb} = +25°C
- V_D = +8V
- V_{G1} = 0V
- V_{G2} = +2V

Symbol	Parameter	Min	Typ	Max	Unit
F	Frequency range	DC		27	GHz
NF	Simulated Noise figure		3.5	5	dB
G	Small signal gain		13		dB
ΔG	Small signal gain flatness		+/-0.5		dB
S11	Input return loss		-12		dB
S22	Output return loss		-12		dB
Bw@3dB	Frequency Bandwidth @3dB		31		GHz
P1dB	Output power @1dB compression		16.5		dBm
P_{SAT}	Saturated output power		19		dBm
TC	Output tap coupler ratio		24		dB
ΔGD	Group delay variation		+/-10		ps
I_D	Drain current		125		mA

Environmental parameters

Symbol	Parameter	Min	Max	Unit
Tst	Storage temperature	-55	+85	°C
Top	Operating temperature	-40	+85	°C

Absolute Maximum Ratings

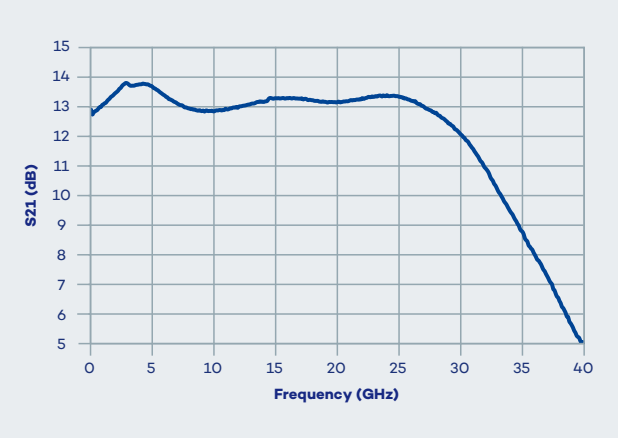
Symbol	Parameter	Min	Max	Unit
V_D	Drain voltage		9	V
V_{G2}	Gate control input access for second stage		V_D/2	V
V_{G1}	Gate control input access for first stage	-1.5	0.15	V
Pin	RF input power		+20	dBm
Pcw	Continuous power dissipation		1.35	W
Tprocess	Temperature process max 20 seconds		+325	°C

Operation of this device above any of these parameters may cause permanent damage.
Care should be taken to avoid supply transient and over voltage. Over voltage above the maximum specified in absolute maximum rating section may cause permanent damage to the device.

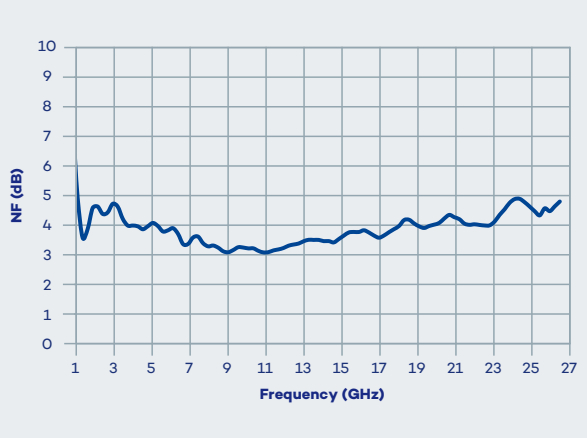
Typical Performance
(Test Under Probes)

Measured assembly: see assembly diagram (except for RF Input and RF Output pads)
Test conditions: unless otherwise noted
- T_{amb} = +25°C
- V_D = +8V
- V_{G1} = 0V, V_{G2} = +2V
- I_D = 125mA

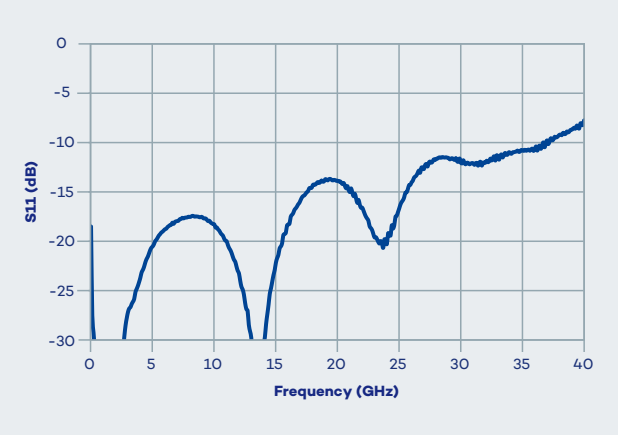
Small Signal Gain



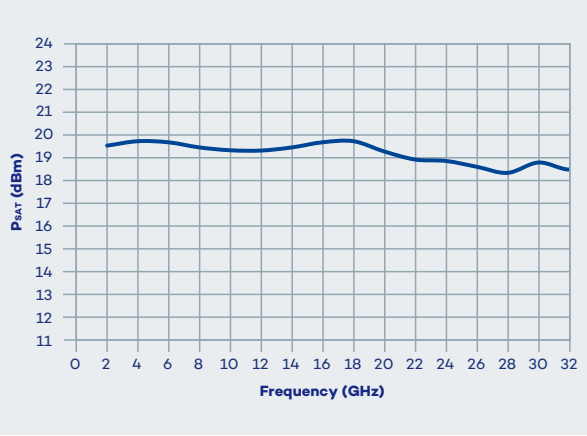
Noise Figure



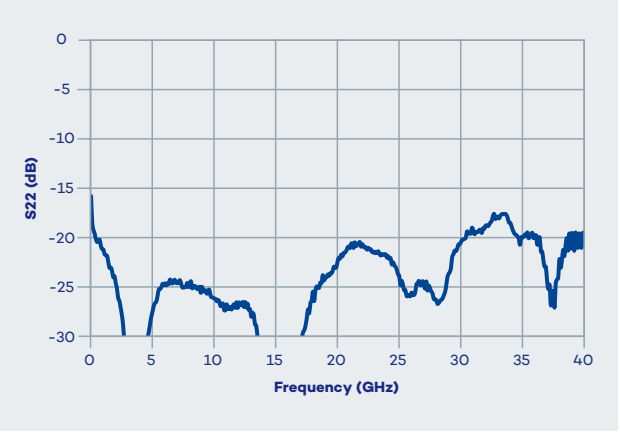
Input Return Loss



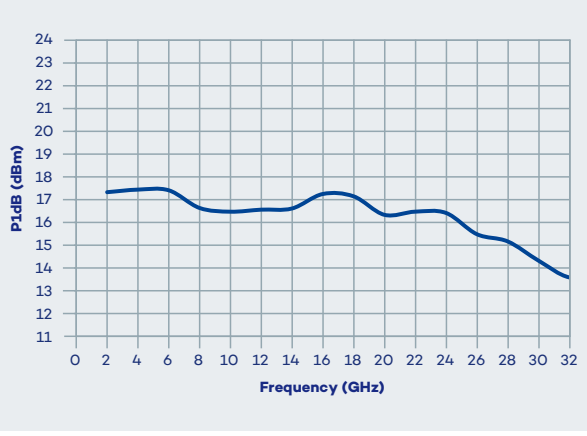
Saturated Output Power



Output Return Loss



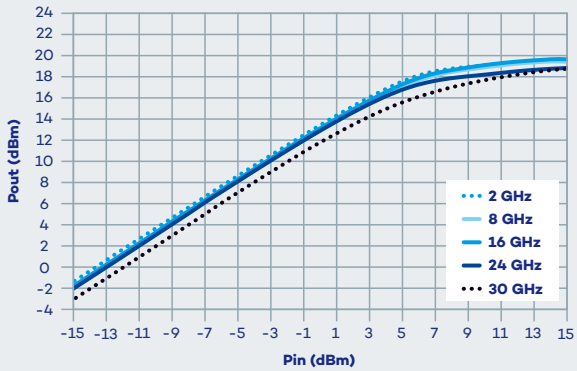
Output P1dB



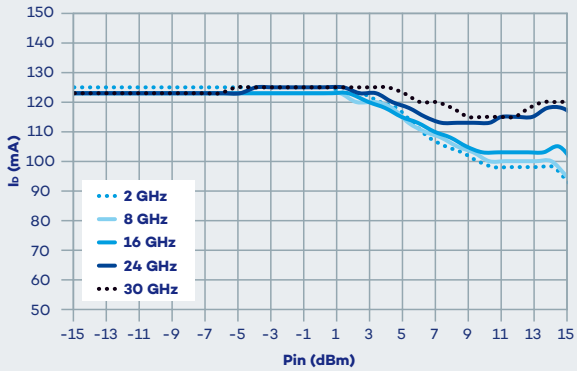
• Typical Performance
(Test Under Probes)

Measured assembly: see assembly diagram (except for RF Input and RF Output pads)
Test conditions: unless otherwise noted
- T_{amb} = +25°C
- V_D = +8V
- V_{G1} = 0V, V_{G2} = +2V
- I_D = 125mA

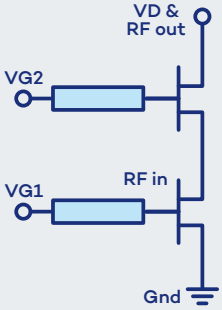
Output Power vs Input Power for various Frequency



Drain Current vs Input Power for various Frequency



Pin description

Pin number	Name	Description	Electrical interface
2	RF in	Amplifier input, this access is DC coupled and internally matched to 50 Ohms.	
4	V_{G2}	Gate control input access for second stage distributed amplifier structure. Apply +2V for nominal biasing conditions.	
5, 6, 7, 8, 9	D0 to D4	Decoupling accesses. These 5 accesses must be connected to a same MIM 100pF or 1000pF capacitor, with a low serial inductance bonding wire.	
18	RF out	RF Amplifier output, this access is DC coupled and internally matched to 50 Ohms . It is also used to bias the drain current (ID), by using a wide bandwidth external Bias-T structure.	
20, 21, 22, 23, 24	G0 to G4	V_{G1} decoupling accesses. These 5 accesses must be connected to V_{G1}	
25	V_{G1}	Gate control input access for first stage distributed amplifier structure. Must be connected to a MIM 100pF or 1000pF capacitor, with a low serial inductance bonding wire. It can also be directly connected to the ground reference plane.	
Die Bottom	Gnd	Die must be connected to RF and DC Ground	

Bias-up procedure

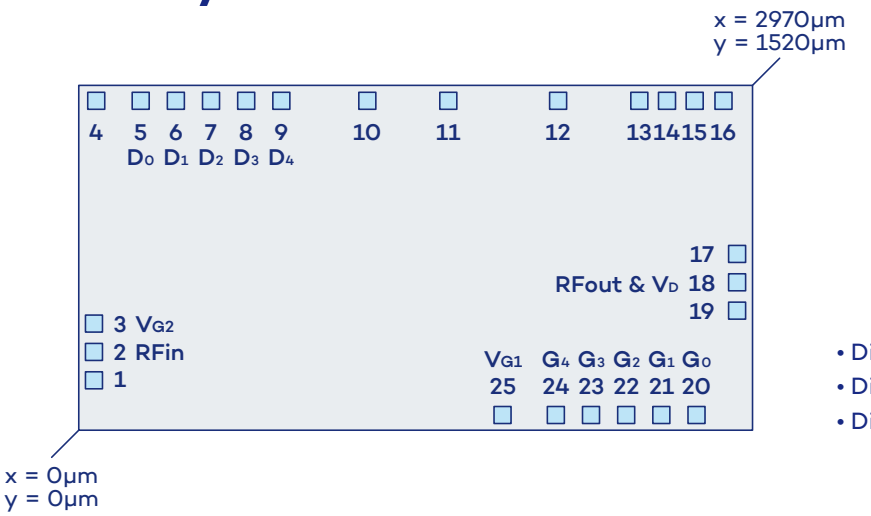
1. Apply V_{G1} = 0V
2. Apply V_D = +8V
3. Apply V_{G2} = +2V
4. Adjust V_{G1} to obtain the specified Drain current ID
5. Turn on RF signal

Bias-down procedure

1. Turn off RF signal
2. Reduce V_{G2} = 0V
3. Reduce V_D = 0V
4. Reduce V_{G1} = 0V

Note : VG1 can be directly connected to the ground, for some application

Die Layout & Pin Out



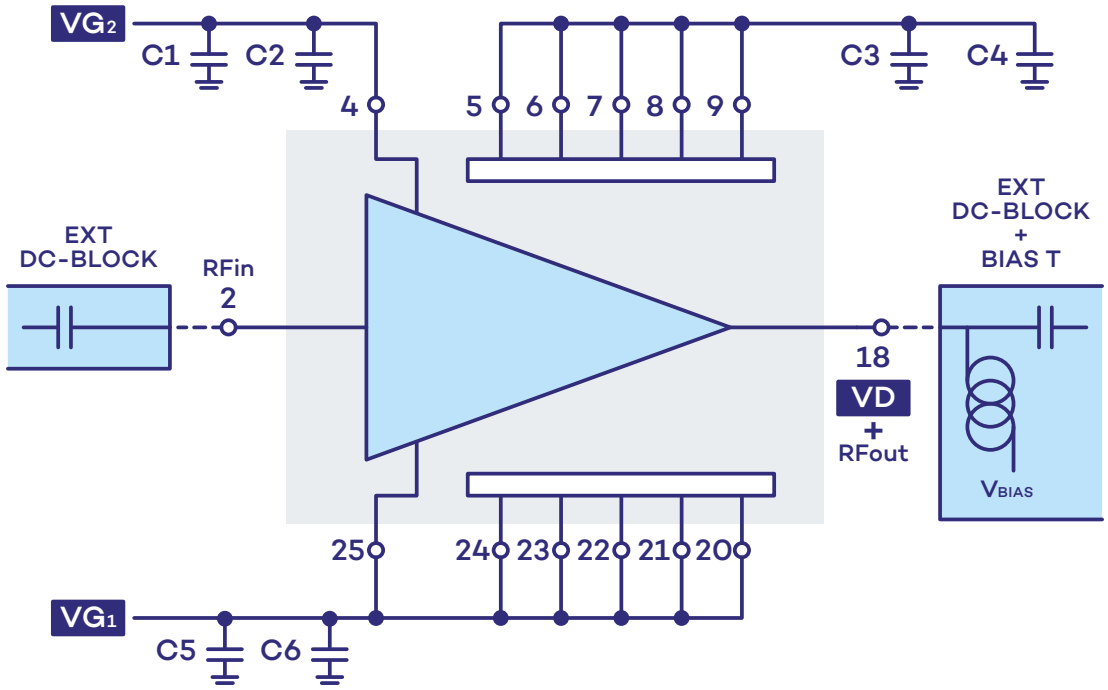
- Die size = 2970µm x 1520µm
- Die thickness = 100µm
- Die size tolerance = 50µm

Pad number	Pad center X (µm)	Pad center Y (µm)	Size (µm x µm)	Name	Function
1	67	220	75 x 75	Gnd	
2	67	345	75 x 75	RFin	RF Input
3	67	470	75 x 75	VG2	Gate Bias
4	77	1452	75 x 75	Gnd	
5	273	1452	75 x 75	D0	
6	428	1452	75 x 75	D1	
7	583	1452	75 x 75	D2	
8	738	1452	75 x 75	D3	
9	893	1452	75 x 75	D4	
10	1272	1452	75 x 75	Reserved	
11	1629	1452	75 x 75	Reserved	
12	2113	1452	75 x 75	Reserved	
13	2471	1452	75 x 75	Reserved	
14	2593	1452	75 x 75	Reserved	
15	2715	1452	75 x 75	Reserved	
16	2842	1452	75 x 75	Reserved	
17	2902	777	75 x 75	Gnd	
18	2902	652	75 x 75	RFout & V_D	RF Output
19	2902	527	75 x 75	Gnd	
20	2723	67	75 x 75	G0	
21	2568	67	75 x 75	G1	
22	2413	67	75 x 75	G2	
23	2258	67	75 x 75	G3	
24	2103	67	75 x 75	G4	
25	1868	67	75 x 75	VG1	Gate Bias

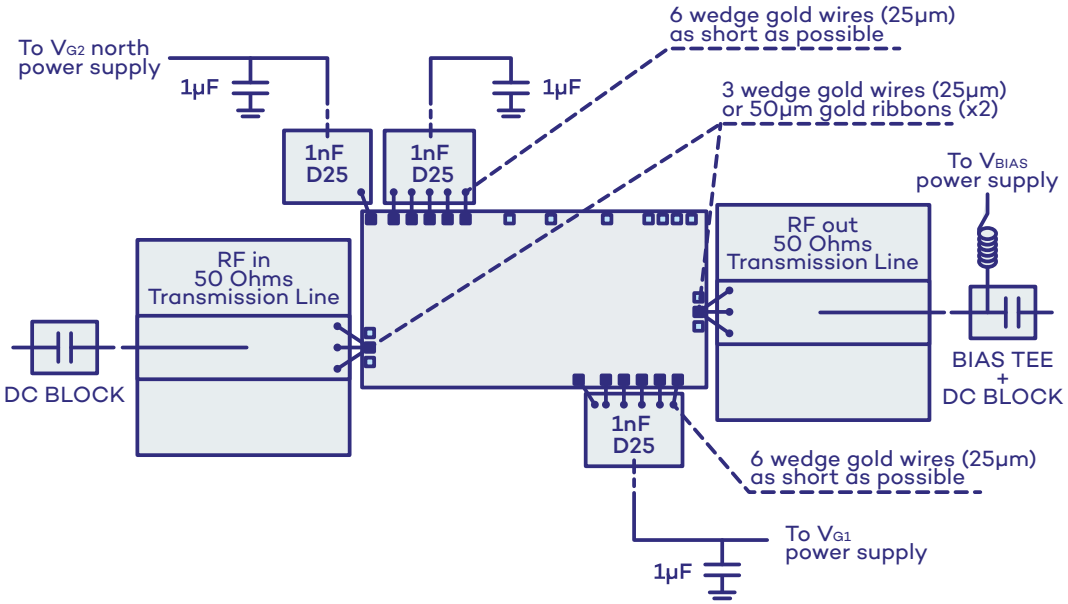
- Die bottom must be connected to ground (RF and DC)

Application circuit

- C1, C4 and C5 = 1µF
- C2, C3 and C6 = 1µF capacitors are MIM type and must be placed as close as possible to the die access.



Typical Assembly Diagram



Ordering information

Product Code	Parameter
VM015D	DC to 27GHz Low Noise Amplifier

Associated Material

- Packaged die
- Die Evaluation Board (die EVB)
- Packaged die Evaluation Board (packaged die EVB)
- Mechanical files (DXF)
- Measurents files (S2P)

Product Compliance Information

Solderability
Use only AuSn (80/20) solder and limit exposure to temperature above 300 °C during 3-4 minutes, maximum.

ESD Sensitivy Rating
Test: Human Body Model (HBM)
Std: JEDEC Standard JESD22-A114

RoHS-Compliance
This part is compliant with EU 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

Other attributes
- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br402) Free
- PFOS Free
- SVHC Free

Contact information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Vectrawave.

vectrawave.com
+33 (0)2 57 63 00 20
sales@vectrawave.com

Vectrawave Device
5, rue de Louis de Broglie
22300 Lannion
France