Vectrawave
RF & Millimeter Wave MMIC Design

DC to 45GHz
Wideband Amplifier

VM025D

General Description

The VM025D is a distributed amplifier designed on a 0.15µm pHEMT process. The device is capable of more than +16dBm of output power at saturation regime, up to 40GHz.

It provides typicaly +14dBm of output power at 1dB of gain compression, with an excellent group delay. The design has been optimized to provide high efficiency. The supply current is as low as 100mA when operating with V_D = +8V.

This device needs a RF output external bias-tee to bias the drain and a RF input external DC-Block.

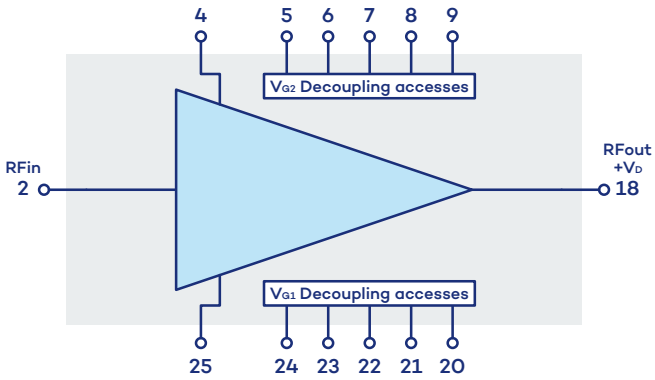
Features

Distributed amplifier pHEMT GaAs MMIC	
Wide band	**DC – 45GHz**
Flat group delay (up to 64Gbps)	
50ΩRF Single ended RF input and output	
DC coupled in, DC coupled out	
P1dB	**+14dBm typ.**
P_{SAT}	**>+16dBm DC to 40GHz**
Small signal gain	**>10dB from DC to 45GHz**
Power supply	**100mA @ +8V**
Chip size	**3.02 x 1.57 x 0.1 (mm)**

Applications

- Wide Band Amplifier
- Radar / ECM / ECCM
- Test and measurement
- Fiber transmission NRZ, PAM4 : 56 / 64 GBPS
- Broadband / datalink communication

Pins Assignement & Functional Block Diagram



Function	Pin number
RF in	2
V_{G2}	4
V_{G2} Decoupling access	5 / 6 / 7 / 8 / 9
RF out & V_D	18
V_{G1} Decoupling access	20 / 21 / 22 / 23 / 24
V_{G1}	25
Gnd	1 / 3 / 17 / 19

Electrical Specifications

Test conditions: unless otherwise noted
- T_{amb} = +25°C
- V_D = +8V
- V_{G1} = 0V
- V_{G2} = +2V

Symbol	Parameter	Min	Typ	Max	Unit
F	Frequency range	DC		45	GHz
NF	Simulated Noise figure		4.5		dB
G	Small signal gain		11		dB
ΔG	Small signal gain flatness		+/-1		dB
S11	Input return loss		-12		dB
S22	Output return loss		-12		dB
P1dB	Output power @1dB compression	11	14		dBm
P_{SAT}	Saturated output power		17		dBm
I_D	Drain current		100		mA

Environmental parameters

Symbol	Parameter	Min	Max	Unit
Tst	Storage temperature	-55	+85	°C
Top	Operating temperature	-40	+85	°C

Absolute Maximum Ratings

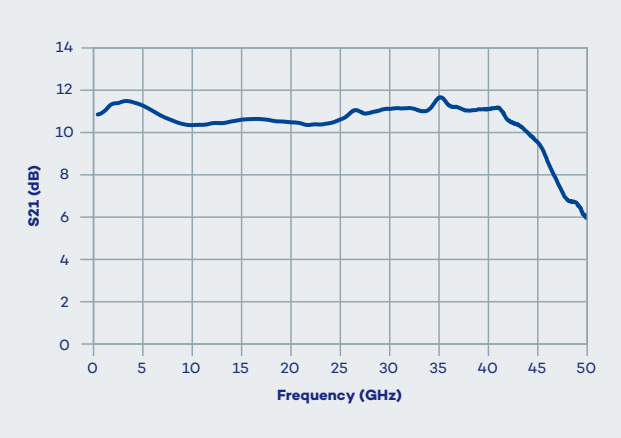
Symbol	Parameter	Min	Max	Unit
V_D	Drain voltage		9	V
V_{G2}	Gate control input access for second stage	-1	V_D/2	V
V_{G1}	Gate control input access for first stage	-1.5	+0.15	V
Pin	RF input power		+20	dBm
Pcw	Continuous power dissipation		1	W
Tprocess	Temperature process max 20 seconds		+325	°C

Operation of this device above any of these parameters may cause permanent damage.

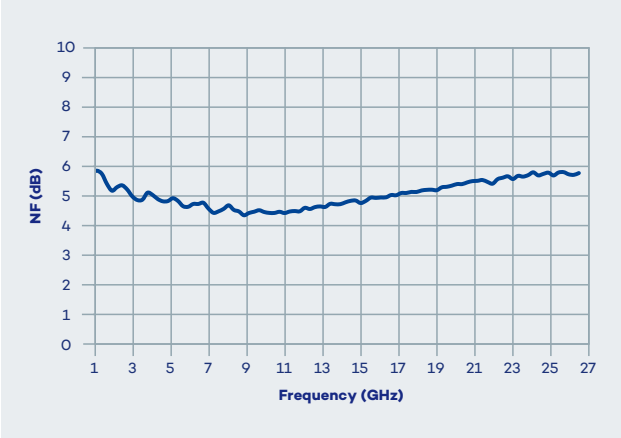
Typical Performance
(Test Under Probes)

Measured assembly: see assembly diagram (except for RF Input and RF Output pads)
- T_{amb} = +25°C
- V_D = +8V
- V_{G1} = 0V, V_{G2} = +2V
- I_D = 100mA

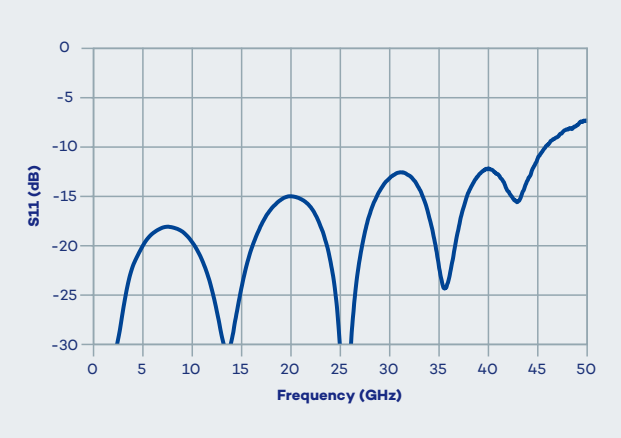
Small Signal Gain



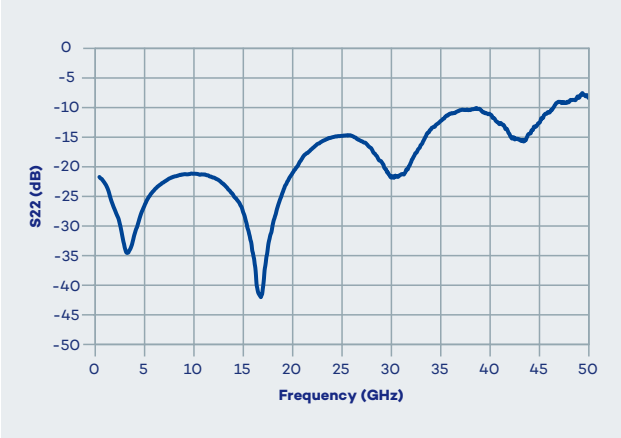
Noise Figure



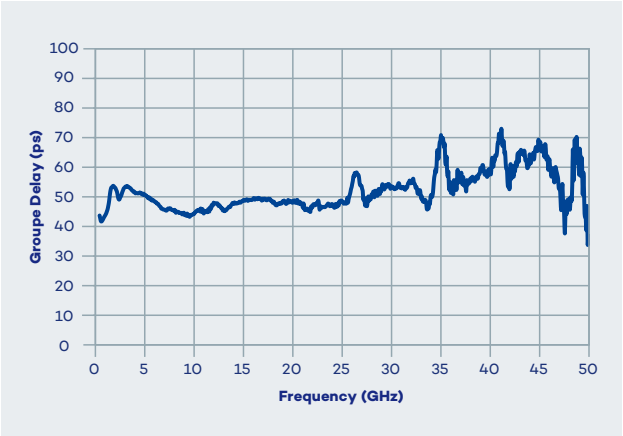
Input Return Loss



Output Return Loss



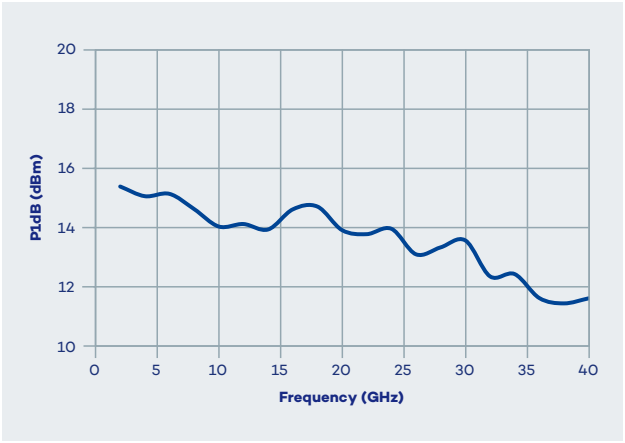
Group Delay



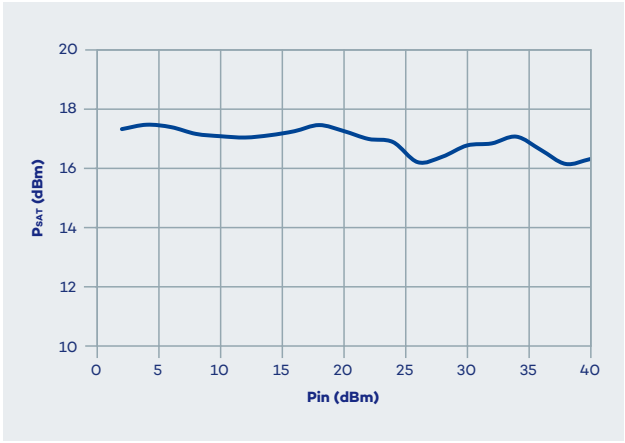
Typical Performance
(Test Under Probes)

Measured assembly: see assembly diagram (except for RF Input and RF Output pads)
- T_{amb} = +25°C
- V_D = +8V
- V_{G1} = 0V, V_{G2} = +2V
- I_D = 100mA

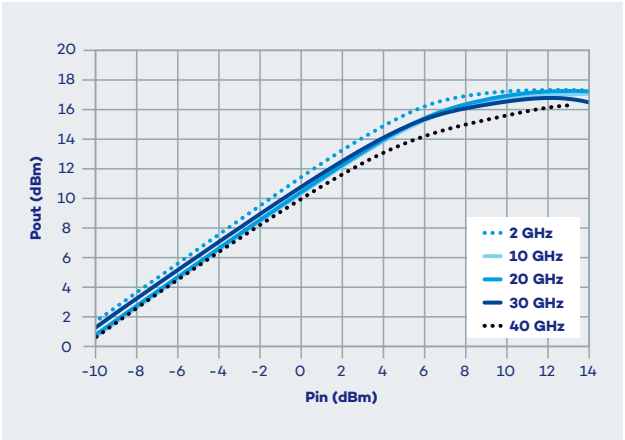
Output P1dB



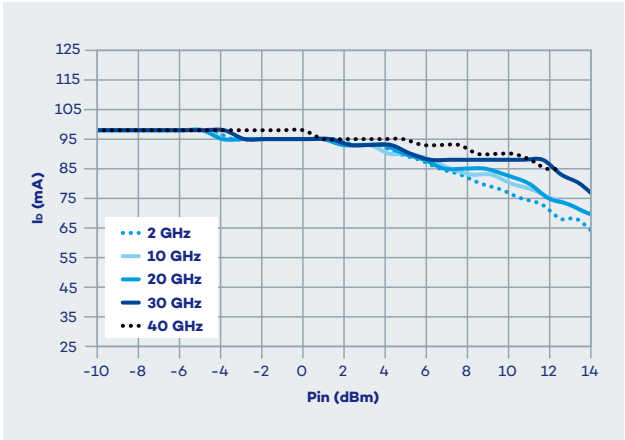
Saturated Output Power



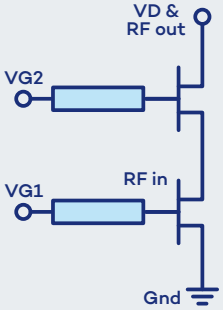
Output power vs Input power vs Frequency



Drain Current vs Input power vs Frequency



Pin description

Pin number	Name	Description	Electrical interface
2	RF in	Amplifier input, this access is DC coupled and internally matched to 50 Ohms.	
4	V_{G2}	Gate control input access for second stage distributed amplifier structure. Apply +2.5V for nominal biasing conditions.	
5, 6, 7, 8, 9	D0 to D4	Decoupling accesses. These 5 accesses must be connected to a same MIM 100pF or 1000pF capacitor, with a low serial inductance bonding wire.	
18	RF out	RF Amplifier output, this access is DC coupled and internally matched to 50 Ohms . It is also used to bias the drain current (I_D), by using a wide bandwidth external Bias-T structure.	
25	V_{G1}	Gate control input access for first stage distributed amplifier structure. Must be connected to a MIM 100pF or 1000pF capacitor, with a low serial inductance bonding wire. It can also be directly connected to the ground reference plane.	
20, 21, 22, 23, 24	G0 to G4	V_{G1} decoupling accesses. These 5 accesses must be connected to V_{G1}	
Die Bottom	Gnd	Die must be connected to RF and DC Ground	

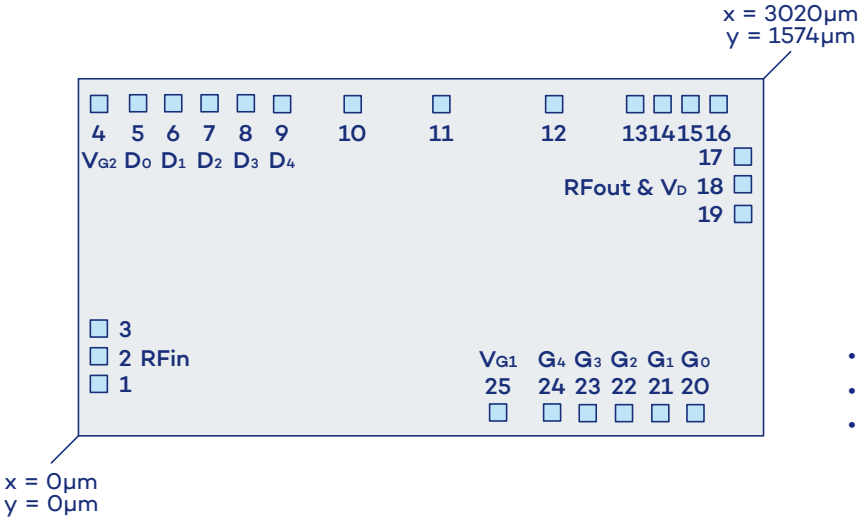
Bias-up procedure

1. Apply V_D = +8V
2. Apply V_{G2} = +2V
5. Turn on RF signal

Bias-down procedure

1. Turn off RF signal
2. Reduce V_{G2} = 0V
3. Reduce V_D = 0V

Die Layout & Pin Out



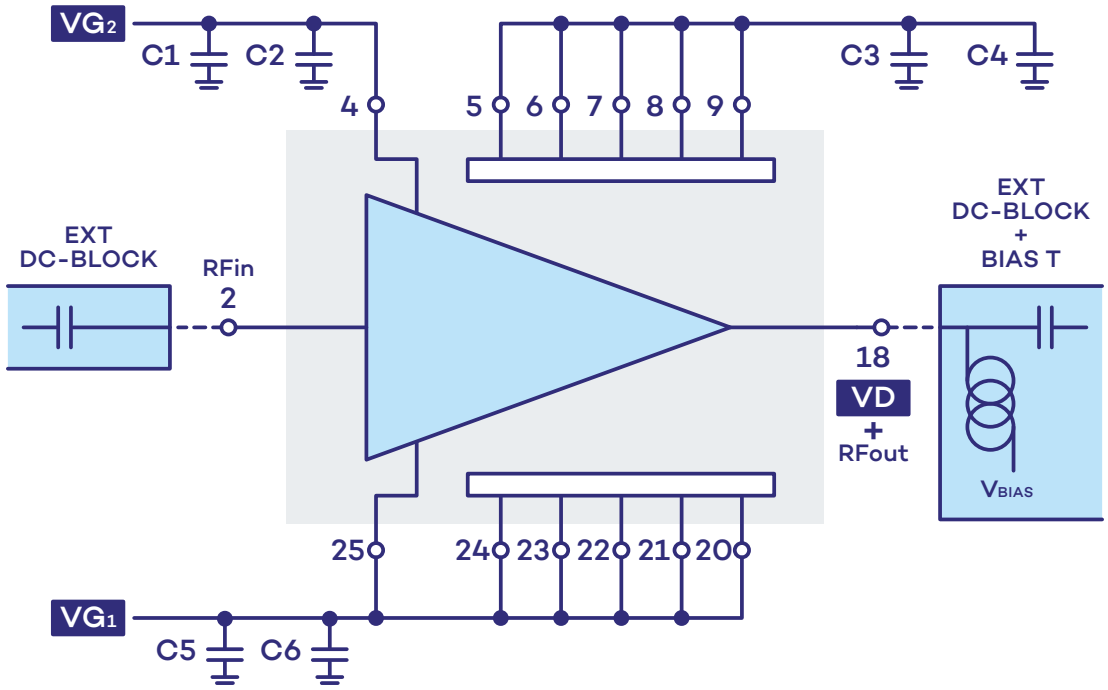
- Die size = 3020µm x 1574µm
- Die thickness = 100µm
- Die size tolerance = 50µm

Pad number	Pad center X (µm)	Pad center Y (µm)	Size (µm x µm)	Name	Function
1	90	229	75 x 75	Gnd	
2	90	351	75 x 75	RFin	RF Input
3	90	473	75 x 75	Gnd	
4	91	1463	75 x 75	V_{G2}	Gate Bias
5	263	1466	75 x 75	D0	
6	418	1466	75 x 75	D1	
7	578	1466	75 x 75	D2	
8	738	1466	75 x 75	D3	
9	898	1462	75 x 75	D4	
10	1209	1462	75 x 75	Reserved	
11	1600	1462	75 x 75	Reserved	
12	2097	1462	75 x 75	Reserved	
13	2454	1462	75 x 75	Reserved	
14	2575	1462	75 x 75	Reserved	
15	2698	1462	75 x 75	Reserved	
16	2828	1462	75 x 75	Reserved	
17	2929	1231	75 x 75	Gnd	
18	2929	1109	75 x 75	RFout & V_D	RF Output
19	2930	978	75 x 75	Gnd	
20	2720	100	75 x 75	G0	
21	2565	100	75 x 75	G1	
22	2405	100	75 x 75	G2	
23	2245	100	75 x 75	G3	
24	2088	103	75 x 75	G4	
25	1850	103	75 x 75	V_{G1}	Gate Bias

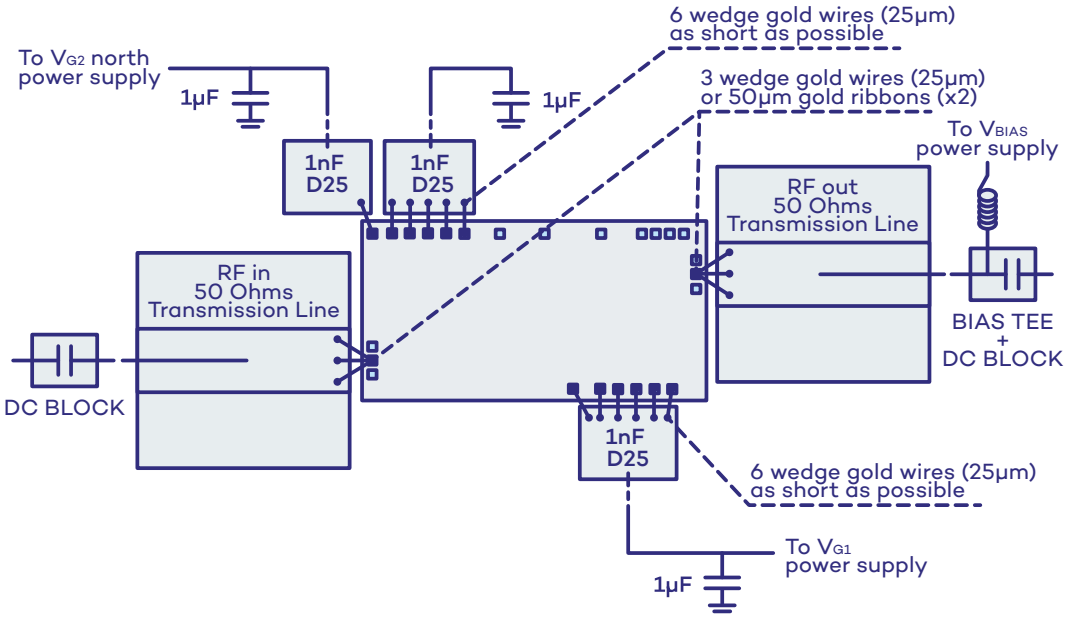
- Die bottom must be connected to ground (RF and DC)

Application circuit

- C1, C4 and C5 = 1µF
- C2, C3 and C6 = 1µF capacitors are MIM type and must be placed as close as possible to the die access.



Typical Assembly Diagram



Ordering information

Product Code	Parameter
VM025D	DC to 45GHz Wideband Amplifier

Associated Material

- Packaged die
- Die Evaluation Board (die EVB)
- Packaged die Evaluation Board (packaged die EVB)
- Mechanical files (DXF)
- Measurents files (S2P)

Product Compliance Information

Solderability
Use only AuSn (80/20) solder and limit exposure to temperature above 300 °C during 3-4 minutes, maximum.

ESD Sensitivy Rating
Test: Human Body Model (HBM)
Std: JEDEC Standard JESD22-A114

RoHS-Compliance
This part is compliant with EU 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

Other attributes
- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br402) Free
- PFOS Free
- SVHC Free

Contact information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Vectrawave.

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