Vectrawave
RF & Millimeter Wave MMIC Design

8 to 12GHz - 25dB- 12W
GaAs Power Amplifier

VM042D

General Description

The VM042D is a 3 Stages analog High Power MMIC amplifier operating in the frequency range 8 to 12GHz. The device is a cascaded 3 stages amplifier designed in 0.25µm pHEMT process. The device is capable of 12W output power at Psat, and provides 25dB of large gain from 8 to 12GHz with less than 1dB of Gain variation.

The design has been optimized to provide high efficiency, supply current is 4.5A with V_D = +8.5V, when delivering 12W output power.

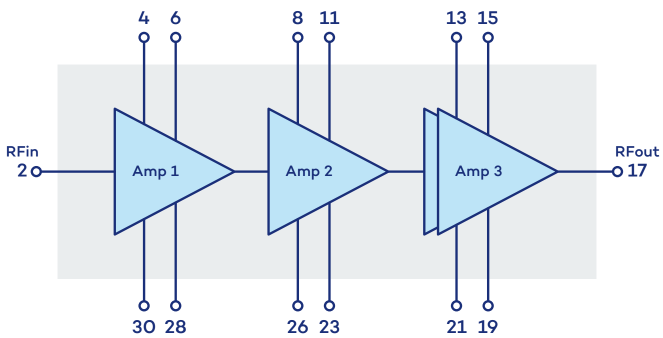
Features

3 stages High Power pHEMT GaAs MMIC	
Wide band	**8 – 12GHz**
High Output P_{SAT}	**12W**
High P1dB	**> +40dBm**
High large signal gain	**25dB typical**
50Ω, AC coupled RF input and output	
Power supply	**4.5A @+8.5V; VG= -0.7V**
Chip size	**4.5 x 3.9 x 0.1 (mm)**

Applications

- X band High Power amplifier
- Broadband communication
- Radar
- Test and measurement

Pins Assignement & Functional Block Diagram



Function	Pin number
RF in	2
V_{G1}	4 / 30
V_{G2}	8 / 26
V_{D1}	6 / 28
V_{D2}	11 / 23
V_{G3}	13 / 21
V_{D3}	15 / 19
RF out	17

Electrical Specifications

Test conditions: unless otherwise noted
- T_{amb} = +25°C
- V_D = +28V
- V_G=-0.7V
- Pulsed mode (pulse width: 10µs, duty cycle: 10%)

Symbol	Parameter	Min	Typ	Max	Unit
F	Frequency range	8		12	GHz
G	Power gain		25		dB
∆G	Gain flatness from 8 to 12GHz		+/-0.7		dB
S11	Input return loss		-10		dB
S22	Output return loss		-10		dB
P_{SAT}	Saturated output power		40.8		dBm
P1dB	Output power @1dB compression		40		dBm
I_{DQ}	Drain quiescent current		3.7		A
I_D Sat	Saturated drain current		4.0	4.6	A
PAE	Power added efficiency		35		%
	Small Signal Gain on 8-10GHz		27		dB
	Small Signal Gain on 10-12GHz		23		dB
	Pout Temperature Coef. {-40°C/+70°C, Pin =+18dBm}			0.01	dB/°C
	Small Signal Gain Temperature Coef. {-40°C/+70°C}		-0.032		dB/°C

Environmental parameters

Symbol	Parameter	Min	Max	Unit
Tst	Storage temperature	-55	+85	°C
Top	Operating temperature	-40	+85	°C

Absolute Maximum Ratings

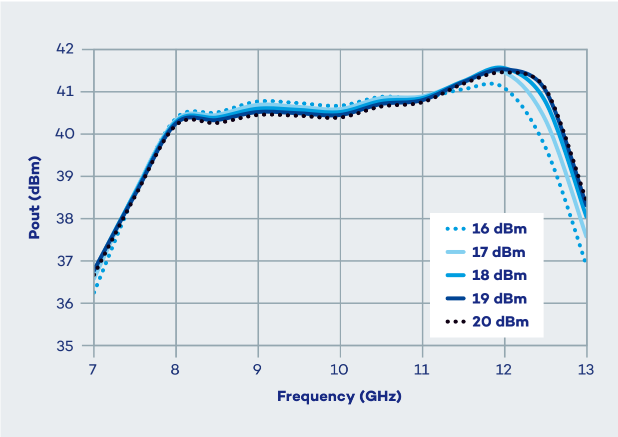
Symbol	Parameter	Min	Max	Unit
V_D	Drain voltage		9	V
V_G	Gate voltage		-0.7	V
Pin	RF input power		+23	dBm
I_D	Drain bias current (I_D = I_{D1} + I_{D2})		4	A
	Soldering temperature (10 seconds max.)		290	°C
Tj	Junction temperature		+150	°C

Care should be taken to avoid supply transient and over voltage. Over voltage above the maximum specified in absolute maximum rating section may cause permanent damage to the device.

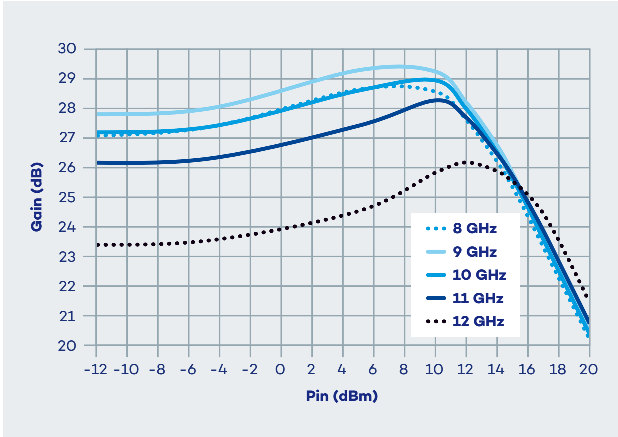
Typical Performance
(Test Under Probes)

Test conditions: unless otherwise noted
- T_{amb} = +25°C
- V_D = +28V
- V_G=-0.7V
- I_D = 4.5A max
- Pulsed mode (pulse width: 10µs, duty cycle: 10%)

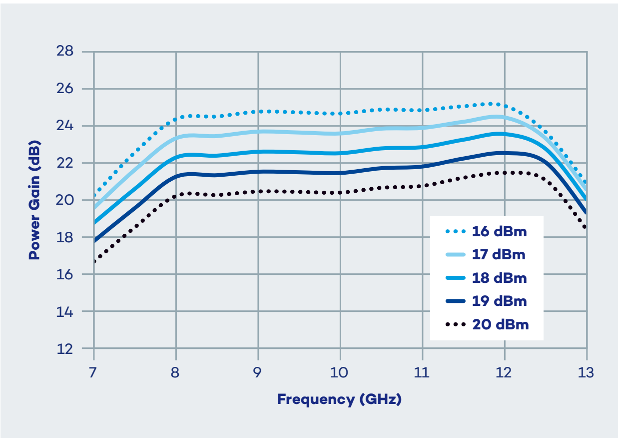
Ouput Power vs Frequency



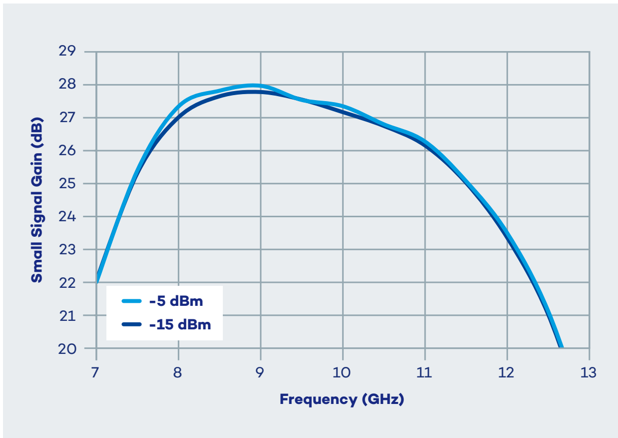
Gain vs Input Power vs Frequency



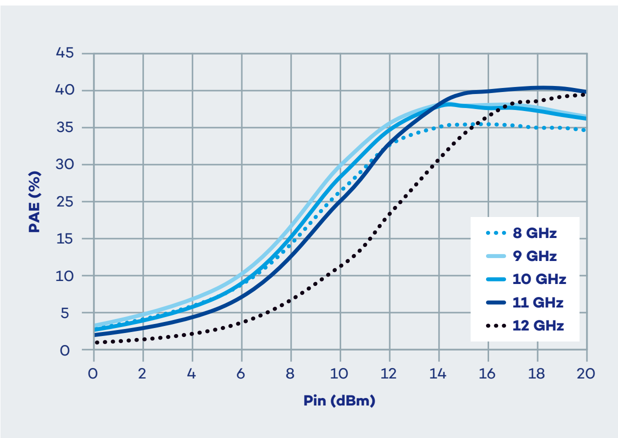
Power Gain vs Frequency vs Input Power



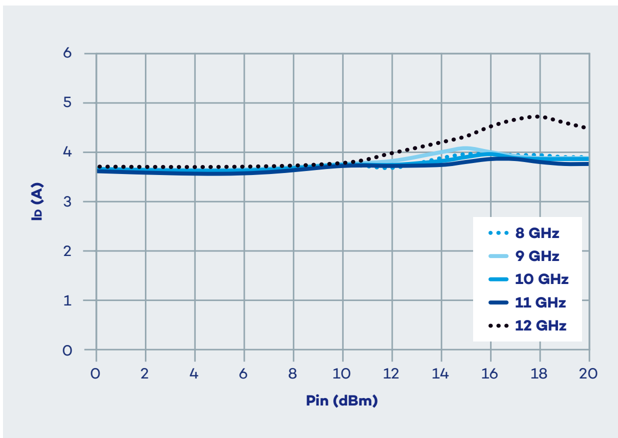
Small Signal Gain vs Frequency



PAE vs Input Power vs Frequency



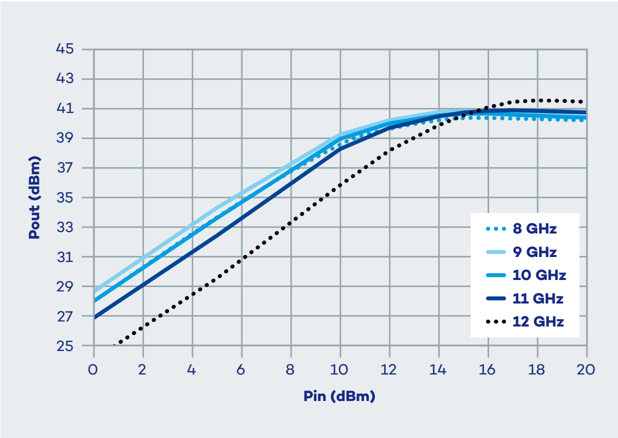
I_D vs Input Power vs Frequency



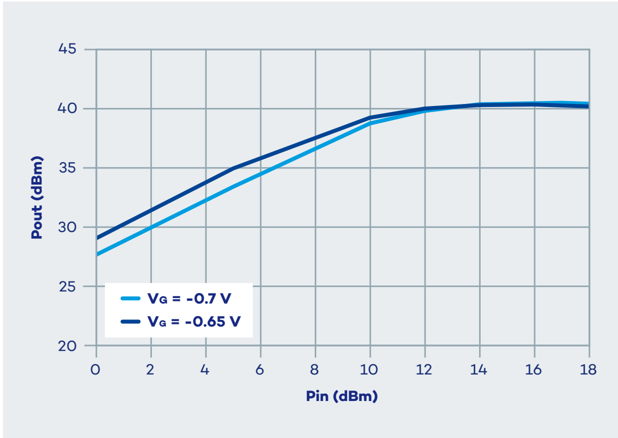
Typical Performance
(Test Under Probes)

Test conditions: unless otherwise noted
- T_{amb} = +25°C
- V_D = +28V
- V_G=-0.7V
- I_D = 4.5A max
- Pulsed mode (pulse width: 10µs, duty cycle: 10%)

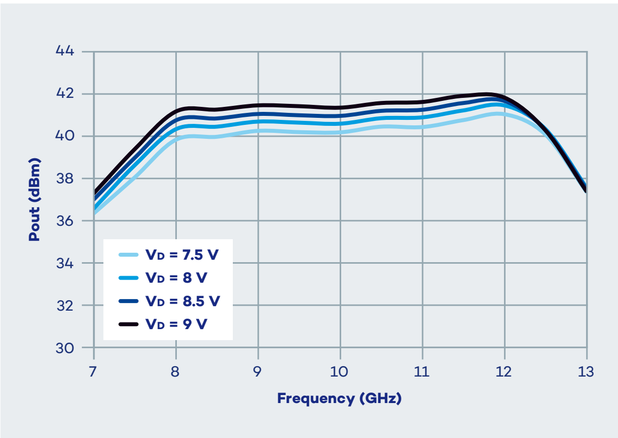
Output Power vs Input Power vs Frequency



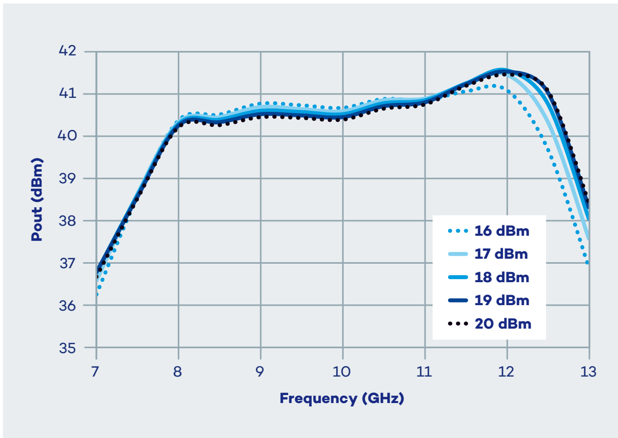
Output Power vs Input Power vs V_G



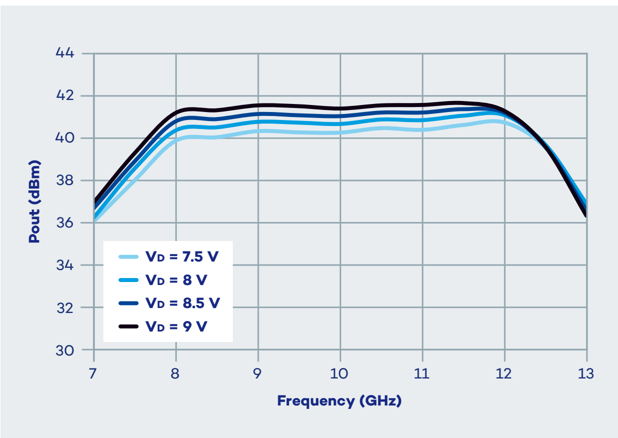
Output Power vs Frequency @17dBm vs V_D



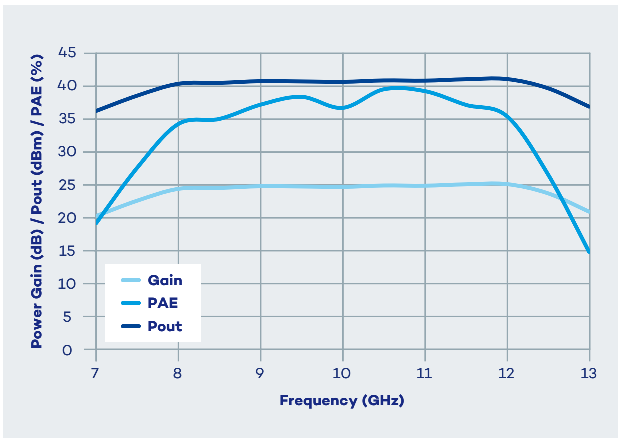
Output Power vs Frequency vs Input Power



Output Power vs Frequency @16dBm vs V_D



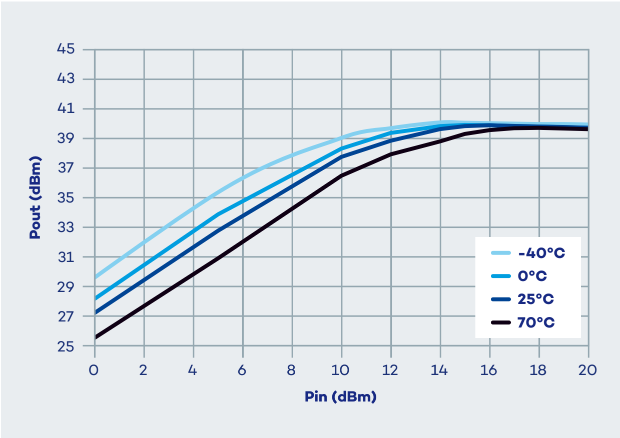
Output Power / Power Gain / PAE vs Frequency



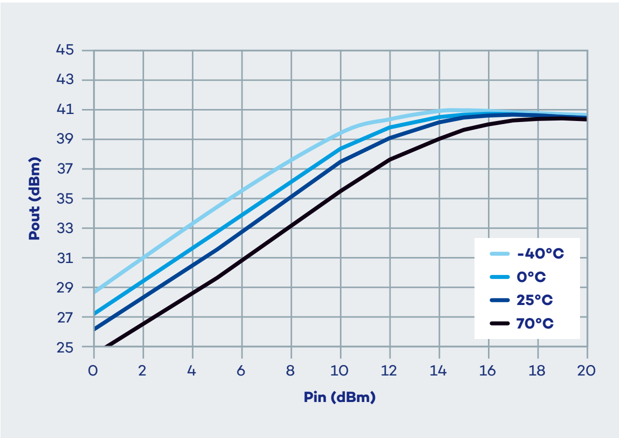
Typical Performance
(Board Measurements)

Test conditions: unless otherwise noted
- T_{amb} = +25°C - using heating cooler
- V_D = +28V
- V_G=-0.7V
- I_D = 4.5A max
- Pulsed mode (pulse width: 10µs, duty cycle: 10%)

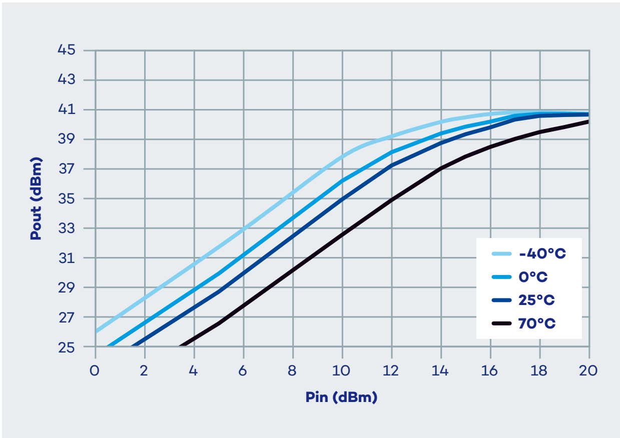
Output Power vs Input Power vs Temperature @ 8GHz



Output Power vs Input Power vs Temperature @ 10GHz



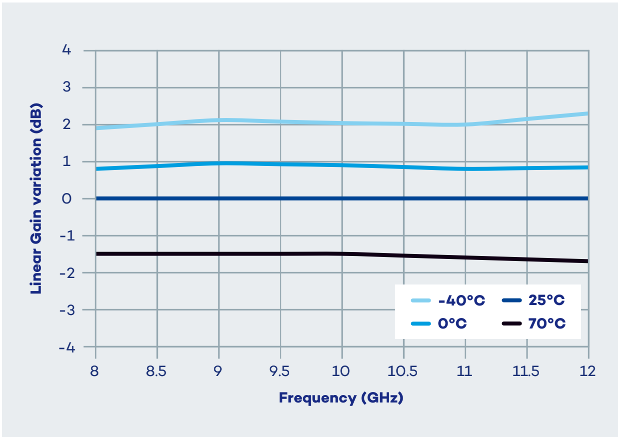
Output Power vs Input Power vs Temperature @ 12GHz



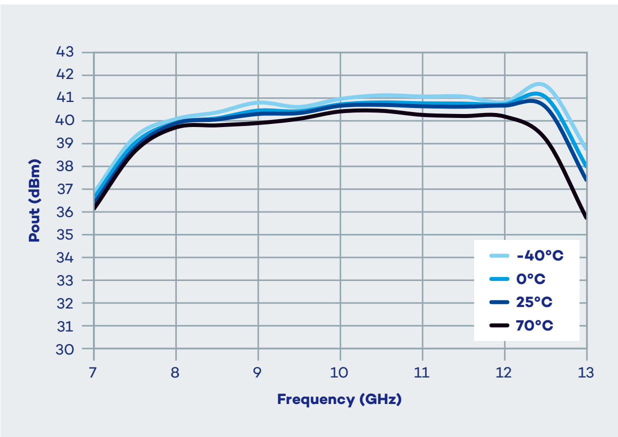
Typical Performance
(Board Measurements)

Test conditions: unless otherwise noted
- T_{amb} = +25°C - using heating cooler
- V_D = +28V
- V_G=-0.7V
- I_D = 4.5A max
- Pulsed mode (pulse width: 10µs, duty cycle: 10%)

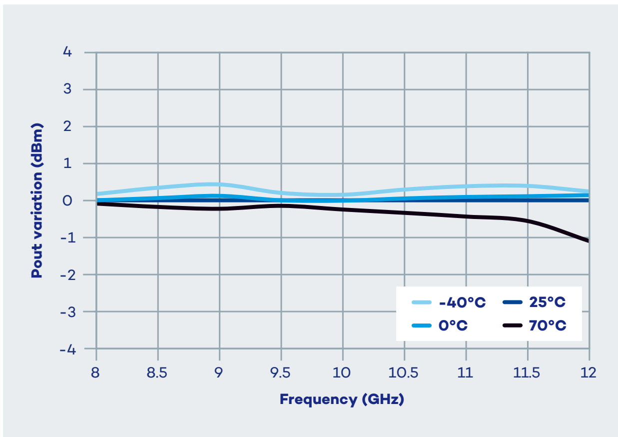
Linear Gain Variation vs Frequency vs Temperature



Input Power vs Frequency vs Temperature

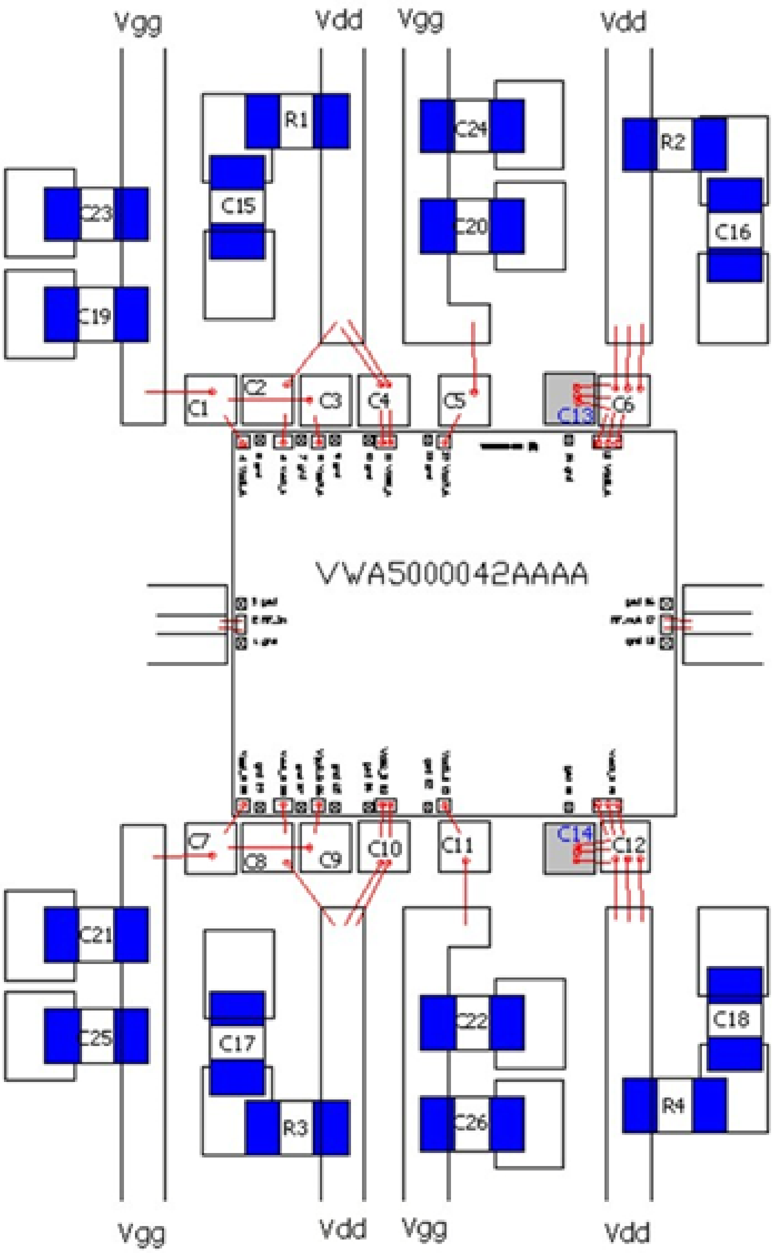


Input Power Variation vs Frequency vs Temperature



Application circuit

- C1 to C12 = 100 pF MIM capacitor close to the die
- C13 and C14 = 10 nF MIM capacitor close to the die
- C15 and C18 = 220 nF
- C19 and C22 = 10nF
- C23 and 26 = 1µF
- R1 to R4 = 11Ω



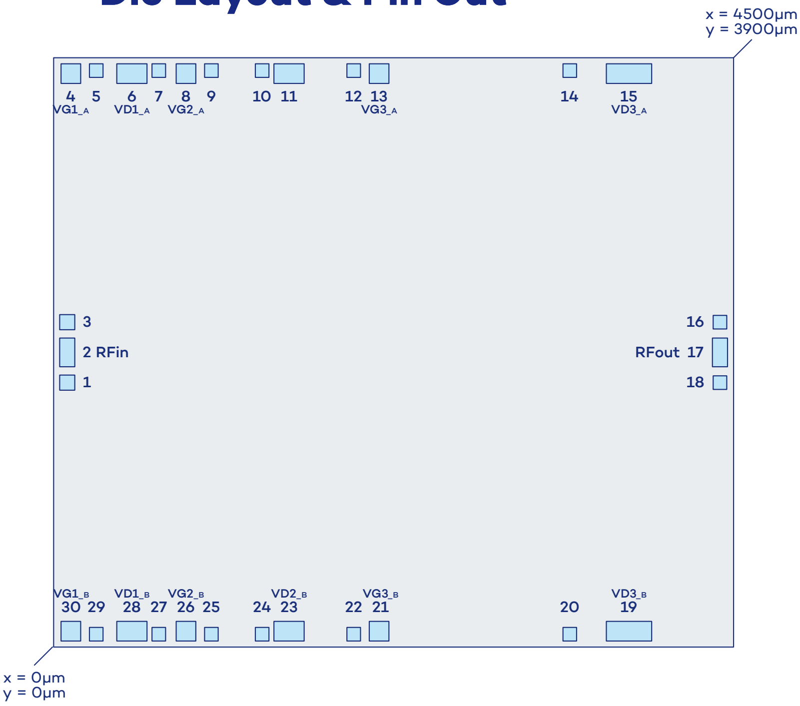
Bias-up procedure

1. Apply V_G = -3V
2. Apply V_D = +28V
3. Adjust V_G = -0.7V
4. Apply RF signal in pulsed mode

Bias-down procedure

1. Turn off RF signal
2. Reduce V_G to -3V
3. Apply V_D = 0V
4. Turn off power supply

Die Layout & Pin Out



- Die size = 4500µm x 3900µm
- Die thickness = 100µm
- Die size tolerance = 50µm

Pad number	Pad center X (µm)	Pad center Y (µm)	Size (µm x µm)	Name	Function
1	90	1750	100 x 100	Gnd	
2	90	1950	100 x 190	RFin	RF Input
3	90	2150	100 x 100	Gnd	
4	114	3795	130 x 130	VG1_A	Gate Bias
5	282	3815	90 x 90	Gnd	
6	518	3795	200 x 130	VD1_A	Drain Bias
7	696	3815	90 x 90	Gnd	
8	876	3795	130 x 130	VG2_A	Gate Bias
9	1044	3815	90 x 90	Gnd	
10	1380	3815	90 x 90	Gnd	
11	1558	3795	200 x 130	VD2_A	Drain Bias
12	1986	3815	90 x 90	Gnd	
13	2154	3795	130 x 130	VG3_A	Gate Bias
14	3416	3815	90 x 90	Gnd	
15	3808	3795	300 x 130	VD3_A	Drain Bias
16	4410	2150	90 x 90	Gnd	
17	4410	1950	100 x 190	RFout	RF Output
18	4410	1750	90 x 90	Gnd	
19	3808	105	300 x 130	VD3_B	Drain Bias
20	3416	85	90 x 90	Gnd	
21	2154	105	130 x 130	VG3_B	Gate Bias
22	1986	85	90 x 90	Gnd	
23	1558	105	200 x 130	VD2_B	Drain Bias
24	1380	85	90 x 90	Gnd	
25	1044	85	90 x 90	Gnd	
26	876	105	130 x 130	VG2_B	Gate Bias
27	696	85	90 x 90	Gnd	
28	518	105	200 x 130	VD1_B	Drain Bias
29	282	85	90 x 90	Gnd	
30	114	105	130 x 130	VG1_B	Gate Bias

- Die bottom must be connected to ground (RF and DC)

Ordering information

Product Code	Parameter
VM042D	8 to 12GHz - 25dB - 12W GaAs Power Amplifier

Associated Material

- Packaged die
- Die Evaluation Board (die EVB)
- Packaged die Evaluation Board (packaged die EVB)
- Mechanical files (DXF)
- Measurents files (S2P)

Product Compliance Information

Solderability
Use only AuSn (80/20) solder and limit exposure to temperature above 300 °C during 3-4 minutes, maximum.

ESD Sensitivy Rating
Test: Human Body Model (HBM)
Std: JEDEC Standard JESD22-A114

CAUTION !
ESD-SENSITIVE DEVICE

RoHS-Compliance
This part is compliant with EU 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

Other attributes
- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br4O2) Free
- PFOS Free
- SVHC Free

Contact information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Vectrawave.

vectrawave.com
+33 (0)2 57 63 00 20
sales@vectrawave.com

Vectrawave Device
5, rue de Louis de Broglie
22300 Lannion
France