Vectrawave
RF & Millimeter Wave MMIC Design

8 to 10.5GHz - 40W
GaN/SiC Power Amplifier

VM088D

General Description

The VM088D is a Microwave Monolithic Integrated Circuit (MMIC) designed in HEMT (High Electron Mobility Transistor) structure for operating frequency range from 8 to 10.5GHz.

The MMIC is developed on 250nm GaN/SiC process and is internally matched through 50Ω RF accesses. It can provide an output power up to 40W and associated power added efficiency of 38% in pulsed mode.

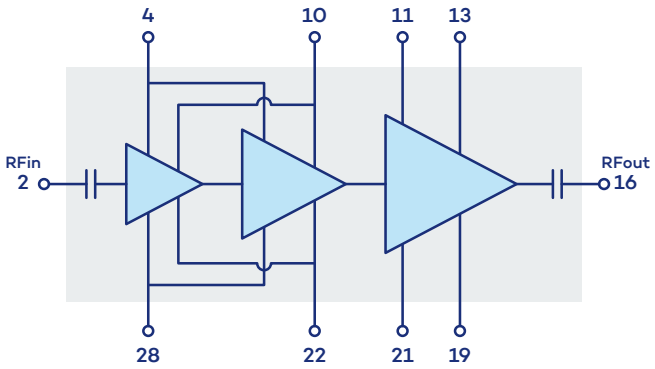
Features

Frequency range	**8 – 10.5GHz**
Output Power	**>46dBm @Pin = 23dBm**
PAE	**38% @Pin = 23dBm**
Linear Gain	**31dB**
DC bias	**V_D = +28V, I_{DQ} = 350mA, V_G = -2.35V (Typical)**
Chip size	**5 x 4.8 x 0.1 (mm)**

Applications

- Radar
- Test and Measurement

Pins Assignement & Functional Block Diagram



Function	Pin number
RF in	2
V_{G1}	4/28
V_{D2}	10/22
V_{G3}	11/21
V_{D3}	13/19
RF out	16

Electrical Specifications

Test conditions: unless otherwise noted
- T_{amb} = +25°C
- V_D = +28V
- I_{DQ} = 350mA (V_G=-2.35V Typ.)
- Pulsed mode (pulse width: 30µs, duty cycle: 10%)

Symbol	Parameter	Min	Typ	Max	Unit
F	Frequency range	8		10.5	GHz
G	Linear gain		31		dB
S11	Input return loss		-10		dB
S22	Output return loss		-12		dB
Pout	Output power (@Pin=23dBm)		46		dBm
PAE	Associated Power Added Efficiency (@Pin=23dBm)		38		%
I_D	Associated Drain current (@Pin=23dBm)		4.3		A
V_D	Drain voltage		28		V

Recommended Operating Conditions

Symbol	Parameter	Value	Unit
V_D	Drain voltage	28	V
I_{DQ}	Drain quiescent current	350	mA
V_G	Gate voltage	-2.35 (Typ.)	V

Absolute Maximum Ratings

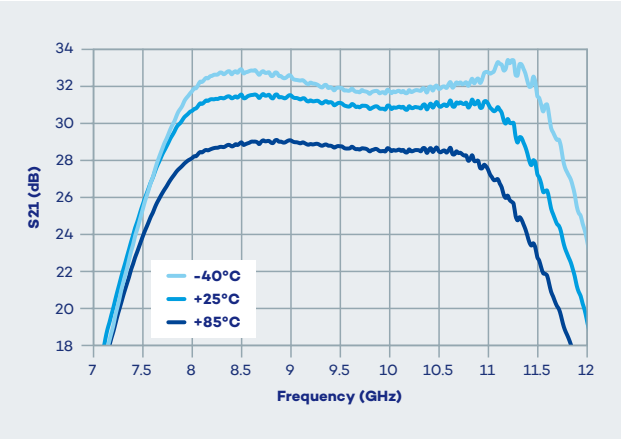
Symbol	Parameter	Value	Unit
V_D	Drain bias voltage	35	V
I_D	Drain bias current	8	A
V_G	Gate bias voltage	-10 to -2	V
Pin	Maximum peak input power overdrive	30	dBm
Tj	Junction temperature	225	°C
Ta	Operating temperature range	-40/+85	°C
Tstg	Storage temperature range	-55/+150	°C

Operation of this device above any of these parameters may cause permanent damage.

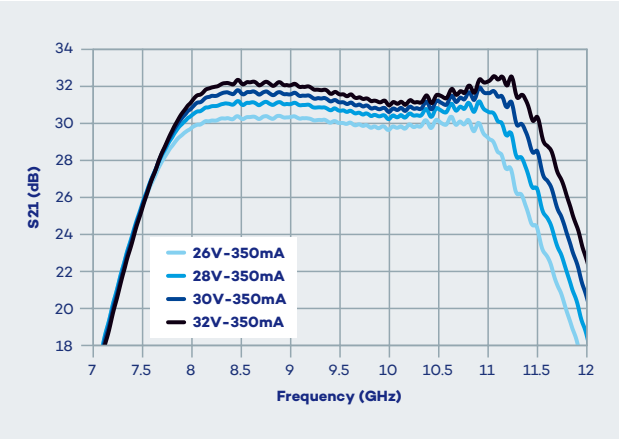
Typical Performance
(Small signal / Board Measurement)

Test conditions: unless otherwise specified
- Reference plane: connector access
- V_D = +28V
- I_{DQ} = 350mA (V_G = -2.35V Typ.)
- Pin = -20dBm

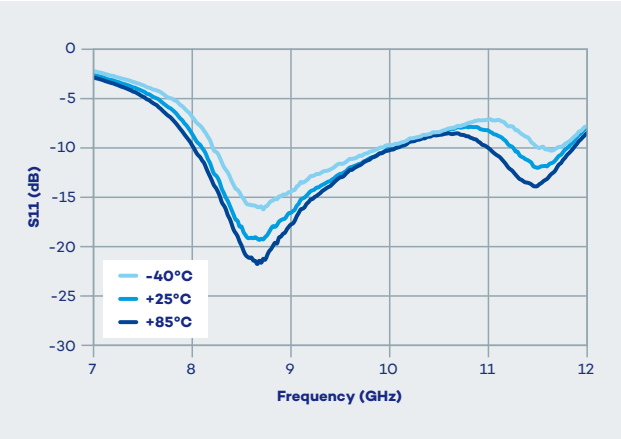
Gain vs Frequency vs Temperature



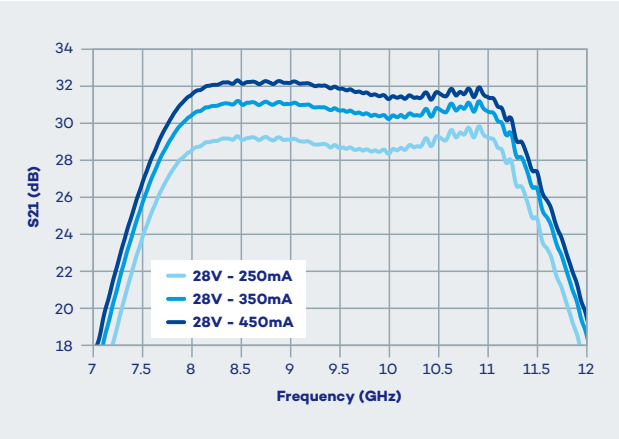
Gain vs Frequency vs V_D



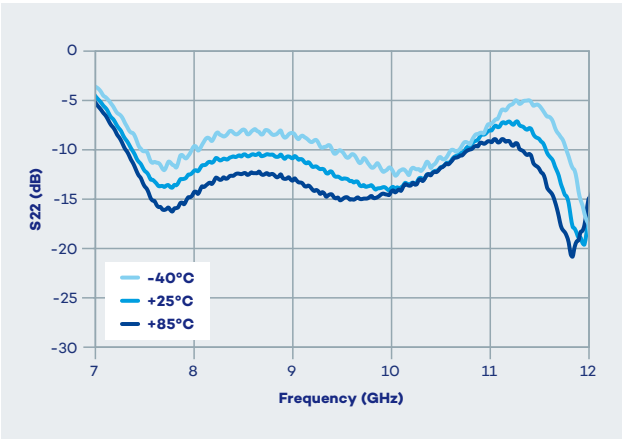
Input Return Loss vs Frequency vs Temperature



Gain vs Frequency vs I_{DQ}



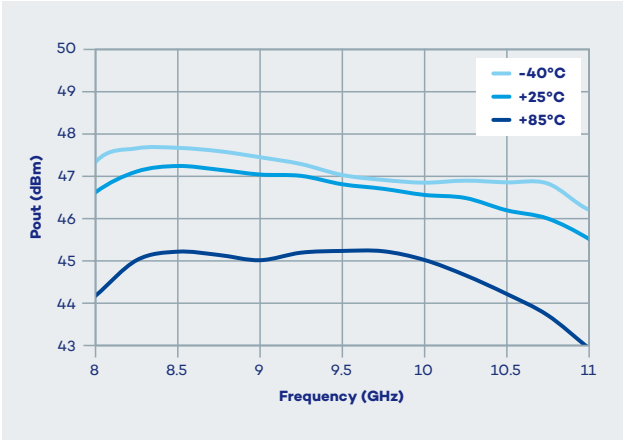
Output Return Loss vs Frequency vs Temperature



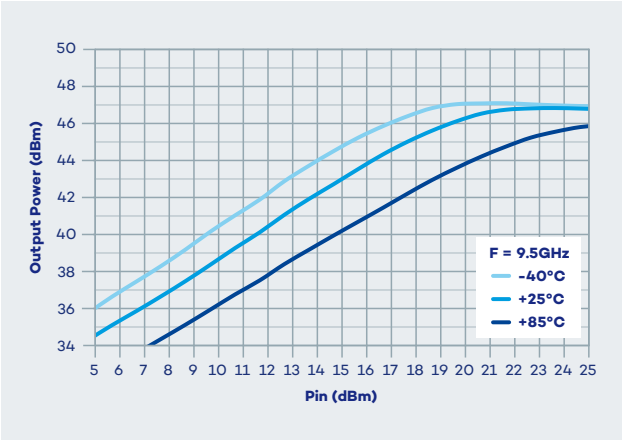
Typical Performance
(Large signal / Board Measurement)

Test conditions: unless otherwise specified
- Reference plane: die access
- V_D = +28V
- I_{DQ} = 350mA (V_G = -2.35V Typ.)
- Pin = +23dBm
- Pulsed mode (pulse width: 30µs, duty cycle: 10%)

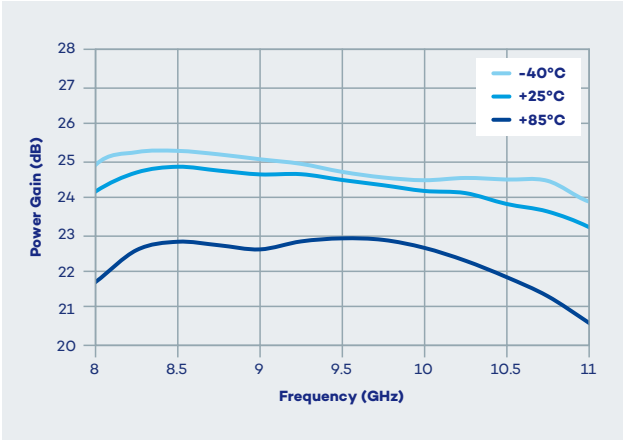
Output Power vs Frequency vs Temperature



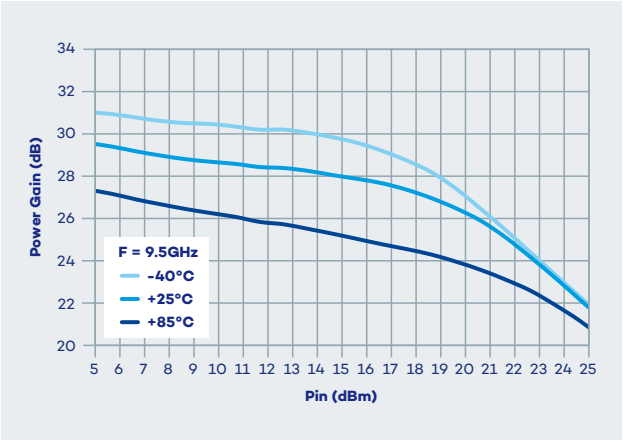
Output Power vs Input Power vs Temperature



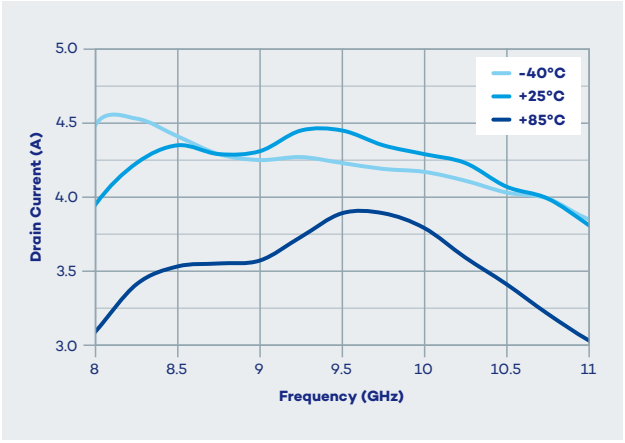
Power Gain vs Frequency vs Temperature



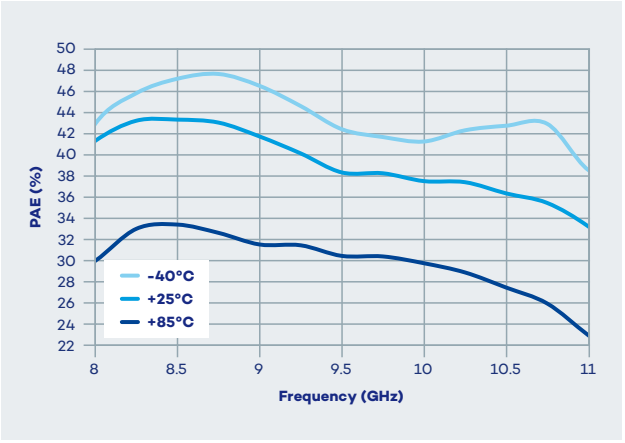
Gain vs Input Power vs Temperature



Drain Current vs Frequency vs Temperature



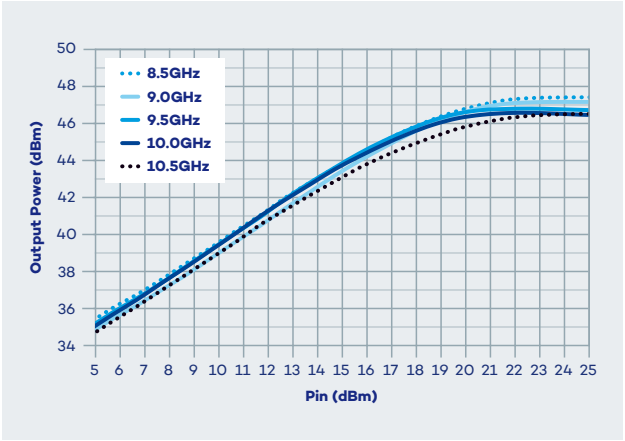
PAE vs Frequency vs Temperature



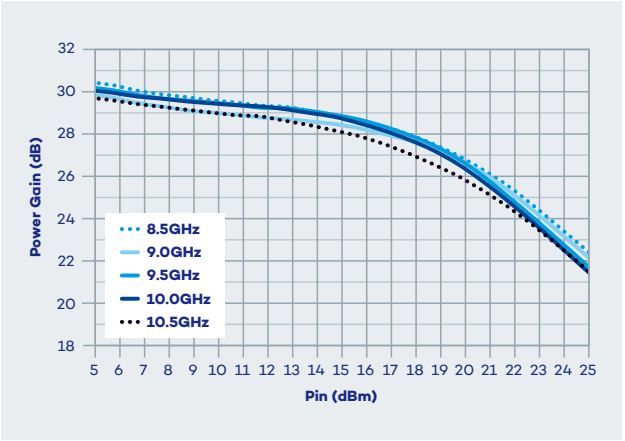
Typical Performance
(Large signal / Board Measurement)

Test conditions: unless otherwise specified
- Reference plane: die access
- V_D = +28V
- I_{DQ} = 350mA (V_G = -2.35V Typ.)
- T_{amb} = +25°C
- Pulsed mode (pulse width: 30µs, duty cycle: 10%)

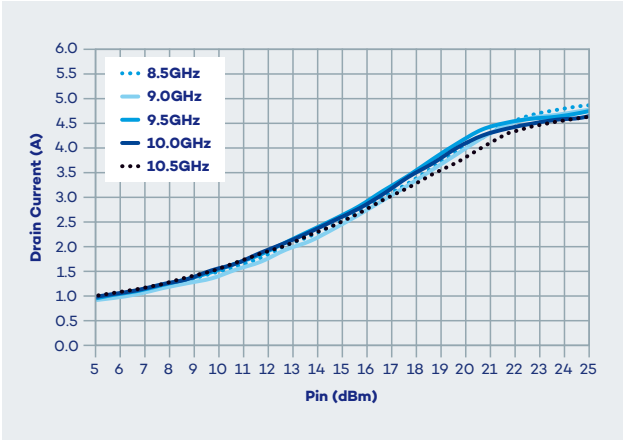
Output Power vs Input Power vs Frequency



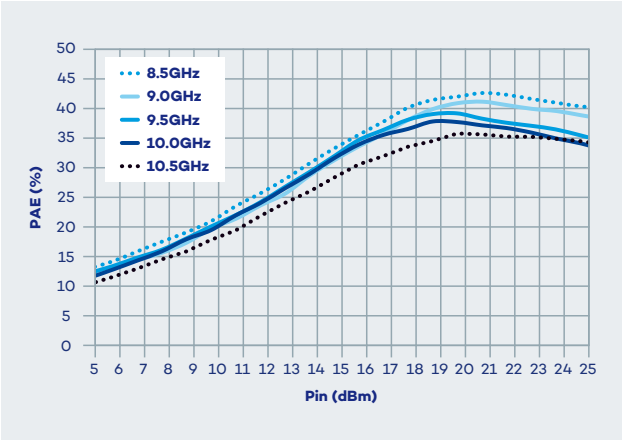
Gain vs Input Power vs Frequency



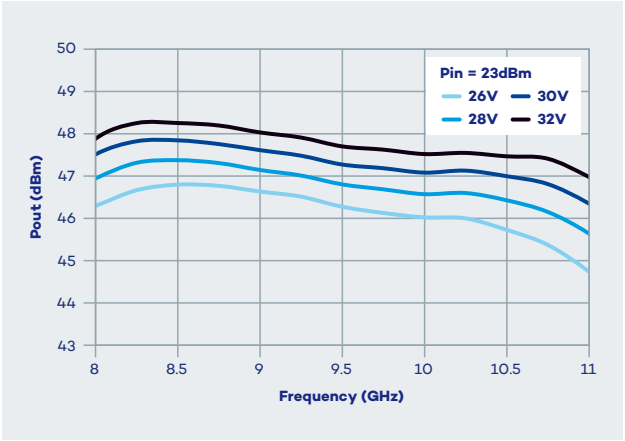
Drain Current vs Input Power vs Frequency



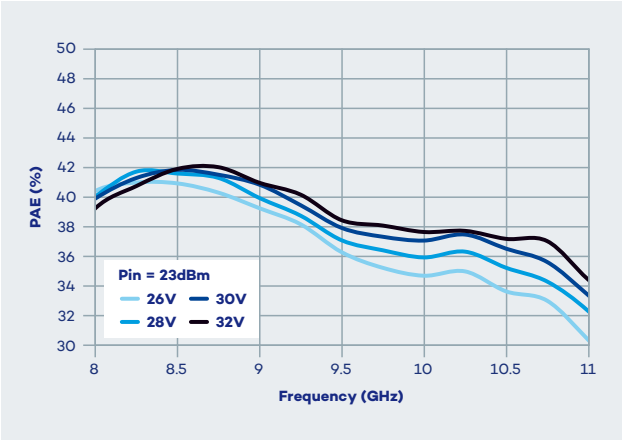
PAE vs Input Power vs Frequency



Output Power vs Frequency vs V_D



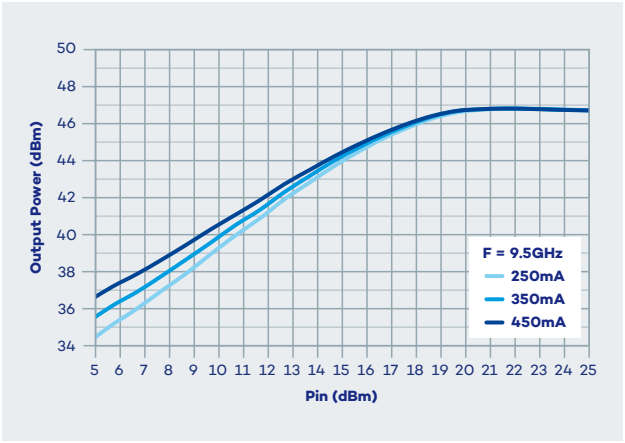
PAE vs Frequency vs V_D



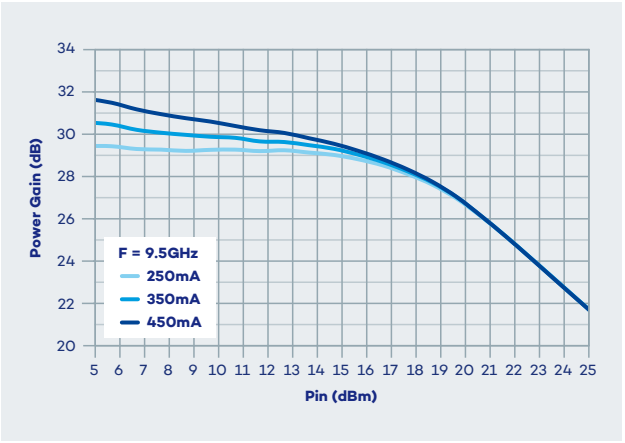
Typical Performance
(Large signal / Board Measurement)

Test conditions: unless otherwise specified
- Reference plane: die access
- V_D = +28V
- T_{amb} = +25°C
- Pulsed mode (pulse width: 30µs, duty cycle: 10%)

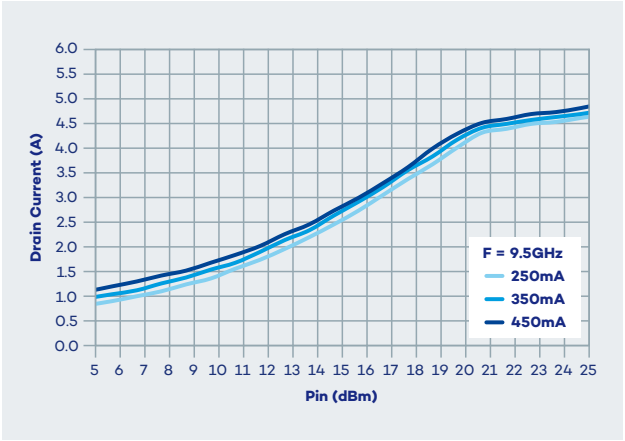
Output Power vs Input Power vs I_{DQ}



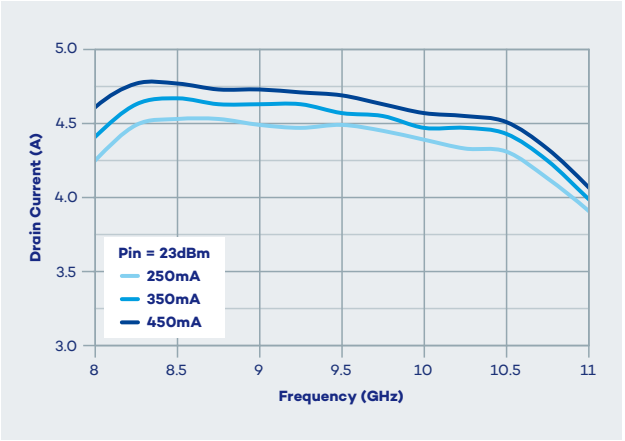
Gain vs Input Power vs I_{DQ}



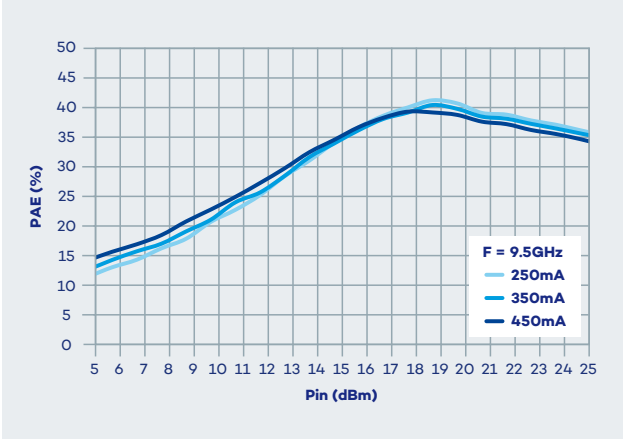
Drain Current vs Input Power vs I_{DQ}



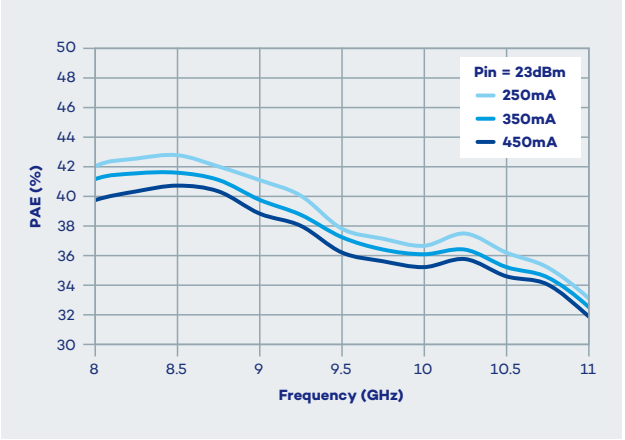
Drain Current vs Frequency vs I_{DQ}



PAE vs Input Power vs I_{DQ}

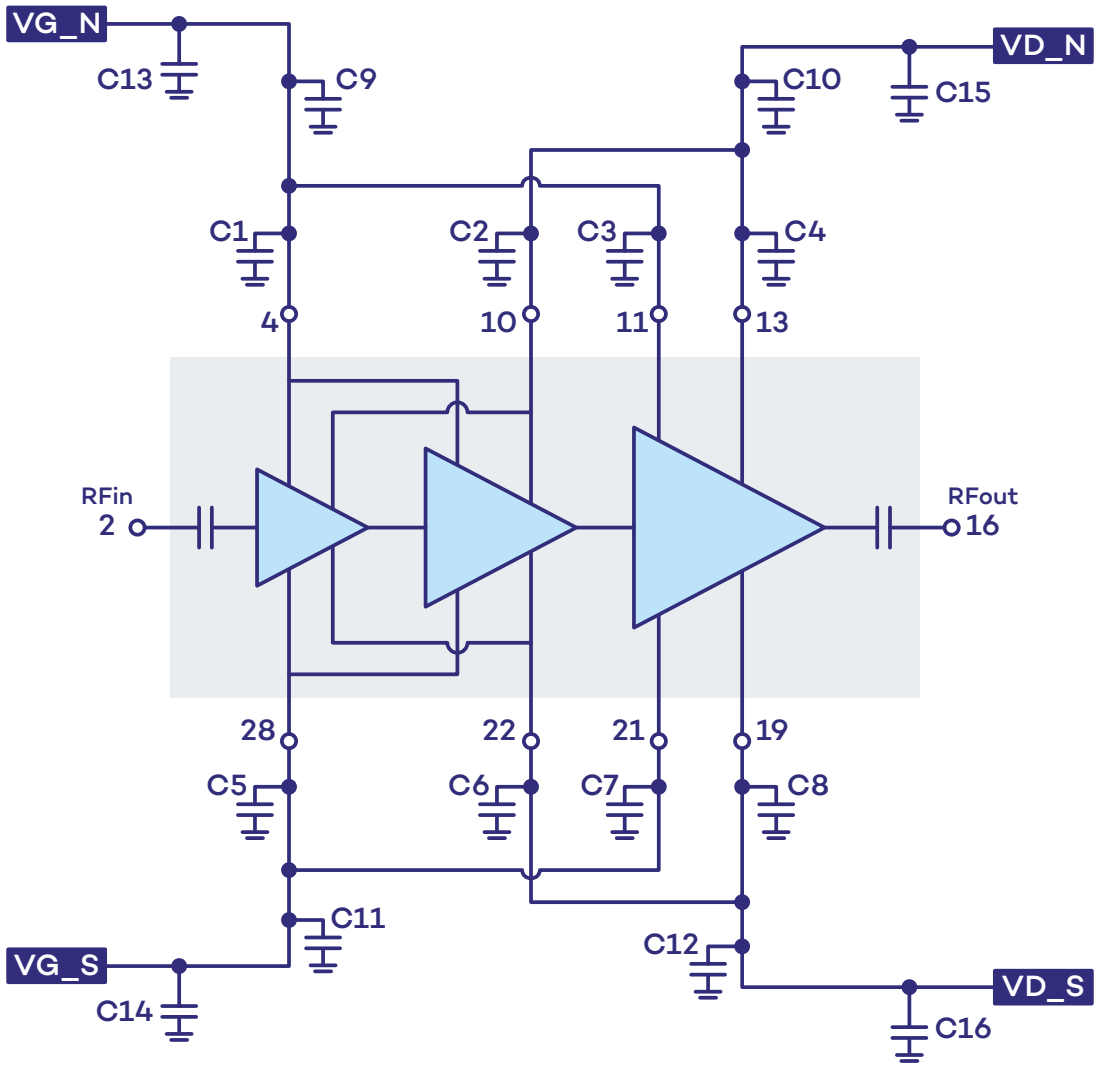


PAE vs Frequency vs I_{DQ}



Application circuit

- C1 to C8 = 1nF
- C9 to C12 = 10nF
- C13 to C16 = 1µF
- C1 to C12 should be MIM capacitors



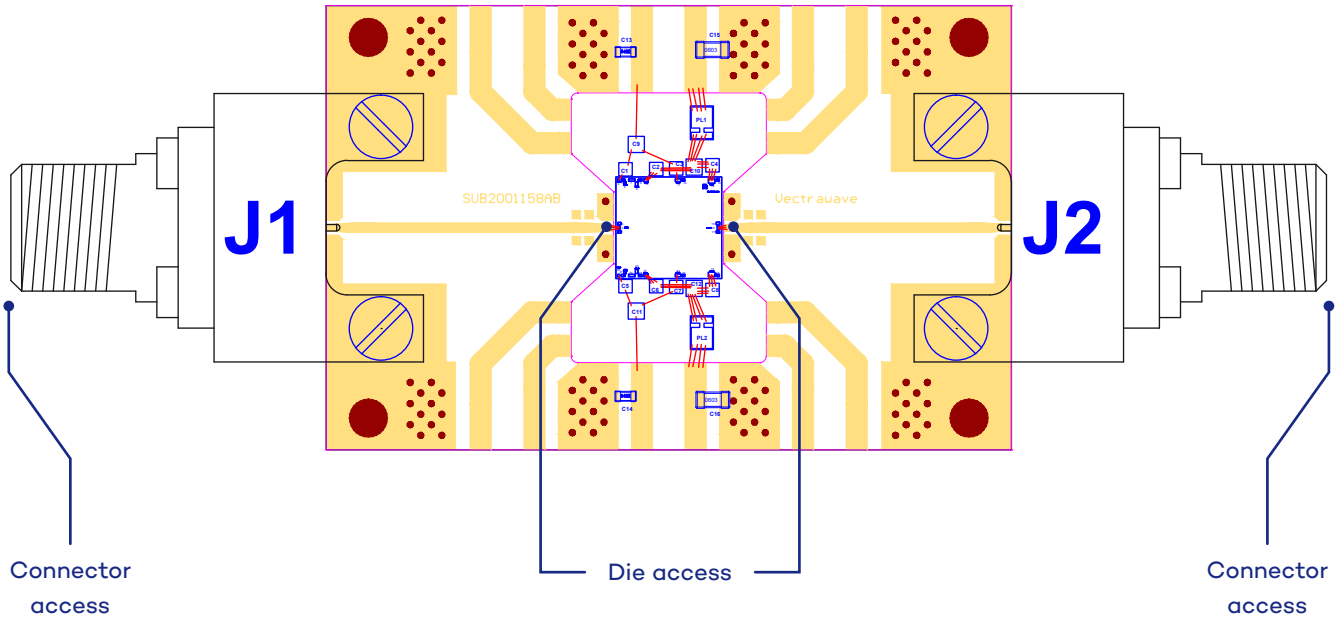
Bias-up procedure

1. Apply V_G = -3V
2. Apply V_D = +28V
3. Increase V_G to obtain the specificied I_{DQ} = 350 mA
4. Apply RF signal

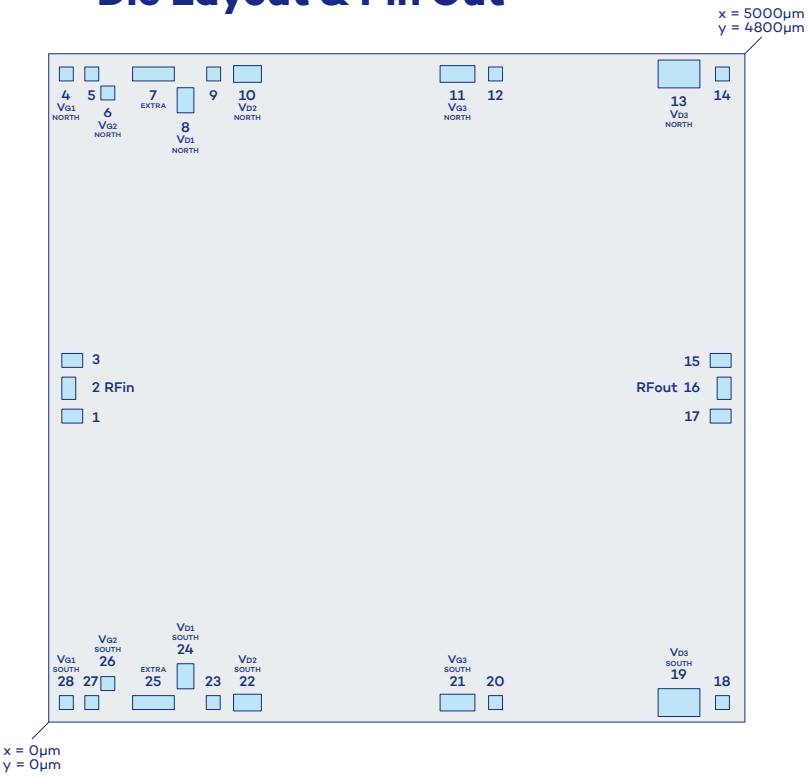
Bias-down procedure

1. Turn off RF signal
2. Reduce V_G to -3V
3. Reduce V_D to +28V
4. Turn off power supply

• Evaluation Board (EVB) Layout Assembly



Die Layout & Pin Out



- Die size = 5000µm x 4800µm
- Die thickness = 100µm
- Die size tolerance = 50µm

Pad number	Pad center X (µm)	Pad center Y (µm)	Size (µm x µm)	Name	Function
1	169.0	2197.5	150 x 100	Gnd	
2	144.0	2397.5	100 x 160	Input	RF Input
3	169.0	2597.5	150 x 100	Gnd	
4	126.6	4654.8	100 x 100	VG1_N	Gate Bias
5	309.2	4654.8	100 x 100	Gnd	
6	424.5	4518.3	100 x 100	VG2_N	Note used
7	752.3	4654.8	300 x 100	Extra	
8	982.5	4465.9	120 x 180	VD1_N	Note used
9	1184.7	4654.8	100 x 100	Gnd	
10	1427.6	4654.8	200 x 120	VD2_N	Drain Bias
11	2936.0	4654.8	250 x 120	VG3_N	Gate Bias
12	3209.2	4654.8	100 x 100	Gnd	
13	4526.9	4654.8	300 x 200	VD3_N	Drain Bias
14	4839.0	4654.8	100 x 100	Gnd	
15	4826.0	2597.5	150 x 100	Gnd	
16	4851.0	2397.5	100 x 160	Output	RF Output
17	4826.0	2197.5	150 x 100	Gnd	
18	4839.0	140.2	100 x 100	Gnd	
19	4526.9	140.2	300 x 200	VD3_S	Drain Bias
20	3209.2	140.2	100 x 100	Gnd	
21	2936.0	140.2	250 x 120	VG3_S	Gate Bias
22	1427.6	140.2	200 x 120	VD2_S	Drain Bias
23	1181.7	140.2	100 x 100	Gnd	
24	982.5	329.1	120 x 180	VD1_S	Note used
25	752.3	140.2	300 x 100	Extra	
26	424.5	276.7	100 x 100	VG2_S	Note used
27	309.2	140.2	100 x 100	Gnd	
28	126.6	140.2	100 x 100	VG1_S	Gate Bias

- VG1_N & VG2_N internally connected
- VG1_S & VG2_S internally connected
- Die bottom must be connected to ground (RF and DC)
- VD1_N & VD2_N internally connected
- VD1_S & VD2_S internally connected

Ordering information

Product Code	Parameter
VM088D	8 to 10.5GHz - 40W GaN/SiC Power Amplifier in die form

Associated Material

- Packaged die
- Die Evaluation Board (die EVB)
- Packaged die Evaluation Board (packaged die EVB)
- Mechanical files (DXF)
- Measurents files (S2P)

Product Compliance Information

Solderability
Use only AuSn (80/20) solder and limit exposure to temperature above 300 °C during 3-4 minutes, maximum.

ESD Sensitivy Rating
Test: Human Body Model (HBM)
Std: JEDEC Standard JESD22-A114

RoHS-Compliance
This part is compliant with EU 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

Other attributes
- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br402) Free
- PFOS Free
- SVHC Free

Contact information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Vectrawave.

vectrawave.com
+33 (0)2 57 63 00 20
sales@vectrawave.com

Vectrawave Device
5, rue de Louis de Broglie
22300 Lannion
France