Vectrawave
RF & Millimeter Wave MMIC Design

8 to 10.75GHz - 50W
GaN/SiC Power Amplifier

VM164D

General Description

The VM164D is a Microwave Monolithic Integrated Circuit (MMIC) designed in HEMT (High Electron Mobility Transistor) structure for operating frequency range of 8 to 10.75GHz.

The MMIC is developed on 250nm GaN/SiC process and is internally matched through 50Ω RF accesses. It can deliver more than 50W of saturated output power and associated power added efficiency of 38% in pulsed mode.

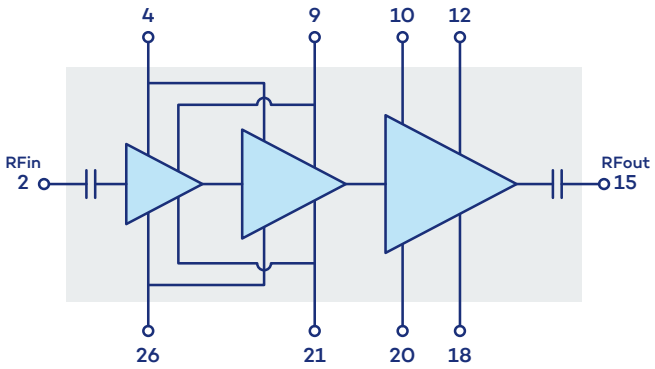
Features

Frequency range	**8 – 10.75GHz**
Output Power	**47dBm @Pin = 25dBm**
PAE	**38% @Pin = 25dBm**
Linear Gain	**30dB**
DC bias	**V_D = +28V, I_{DQ} = 450mA, V_G = -2.35V (Typical)**
Chip size	**5 x 4.8 x 0.1 (mm)**

Applications

- Radar
- Test and Measurement

Pins Assignement & Functional Block Diagram



Function	Pin number
RF in	2
$V_{G1, 2}$	4 / 26
$V_{D1, 2}$	9 / 21
V_{G3}	10 / 20
V_{D3}	12 / 18
RF out	15

Electrical Specifications

Test conditions: unless otherwise noted
- T_{amb} = +25°C
- V_D = +28V
- I_{DQ} = 450mA (V_G=-2.35V Typ.)
- Pulsed mode (pulse width: 100µs, duty cycle: 10%)

Symbol	Parameter	Min	Typ	Max	Unit
F	Frequency range	8		10.75	GHz
G	Linear gain		30		dB
S11	Input return loss		-10		dB
S22	Output return loss		-10		dB
Pout	Output power (@Pin=25dBm)		47.5		dBm
PAE	Associated Power Added Efficiency (@Pin=25dBm)		38		%
I_D	Associated Drain current (@Pin=25dBm)		5.3		A
V_D	Drain voltage		28		V

Recommended Operating Conditions

Symbol	Parameter	Value	Unit
V_D	Drain voltage	28	V
I_{DQ}	Drain quiescent current	450	mA
V_G	Gate voltage	-2.35 (Typ.)	V

Absolute Maximum Ratings

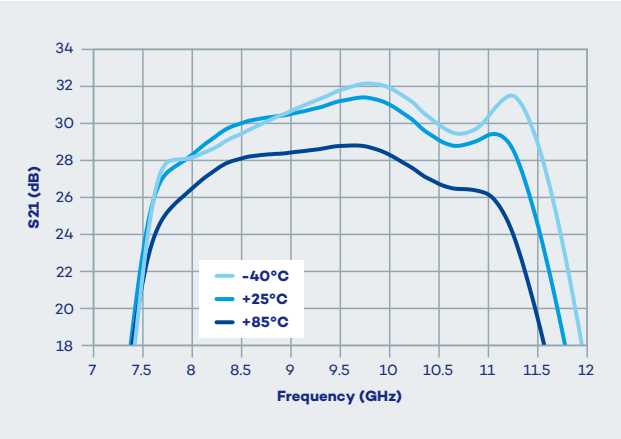
Symbol	Parameter	Value	Unit
V_D	Drain bias voltage	35	V
I_D	Drain bias current	8	A
V_G	Gate bias voltage	-10 to -2	V
Pin	Maximum peak input power overdrive	30	dBm
Tj	Junction temperature	225	°C
Ta	Operating temperature range	-40/+85	°C
Tstg	Storage temperature range	-55/+150	°C

Operation of this device above any of these parameters may cause permanent damage.

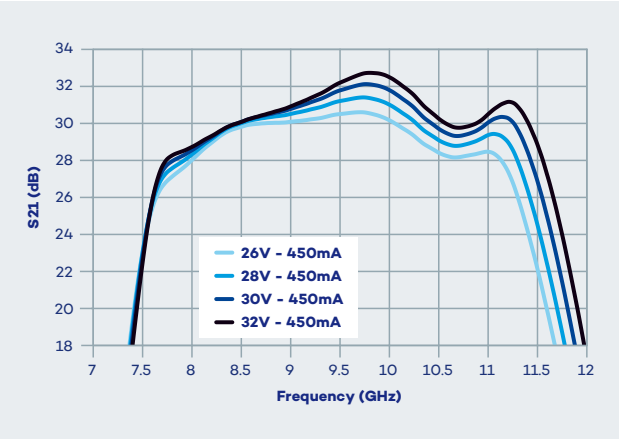
Typical Performance
(Small signal / Board Measurement)

Test conditions: unless otherwise noted
- Reference plane: connector access
- V_D = +28V
- I_{DQ} = 450mA (V_G = -2.35V Typ.)
- Pin = -20dBm

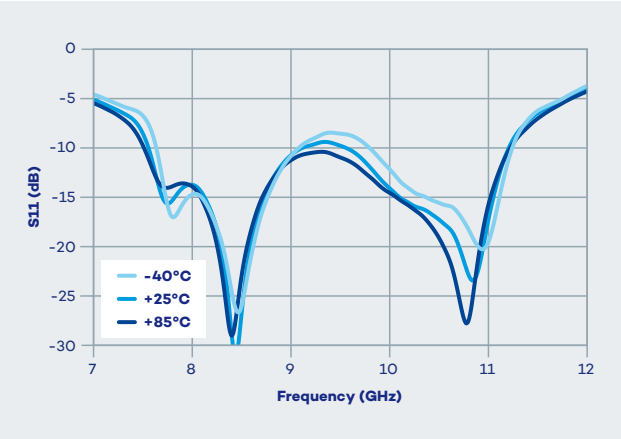
Gain vs Frequency vs Temperature



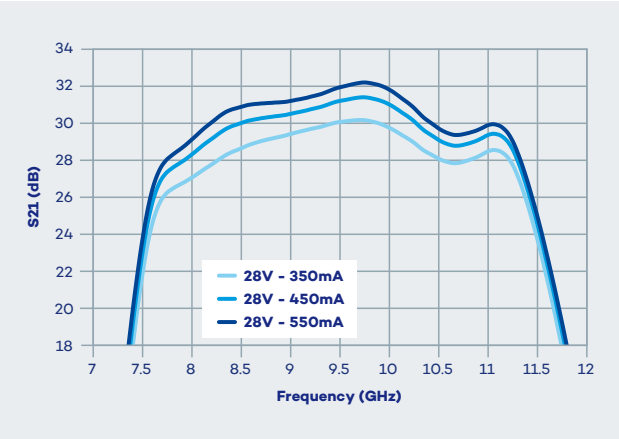
Gain vs Frequency vs V_D



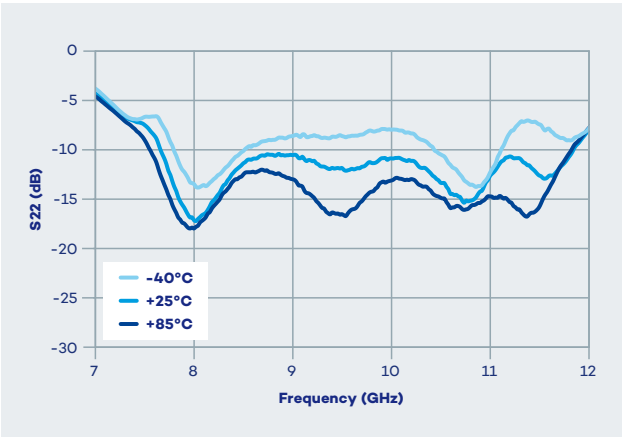
Input Return Loss vs Frequency



Gain vs Frequency vs I_{DQ}



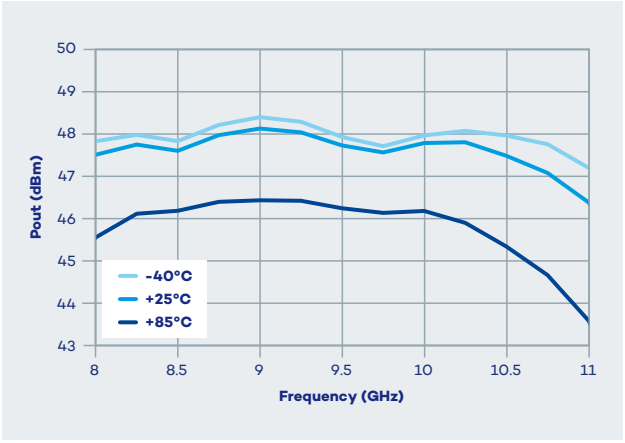
Output Return Loss vs Frequency



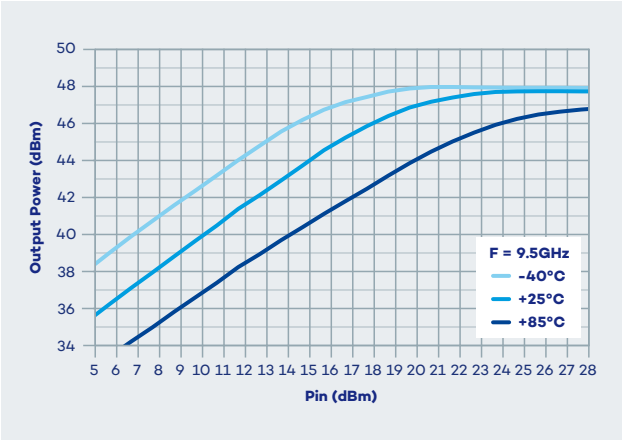
Typical Performance
(Large signal / Board Measurement)

Test conditions: unless otherwise noted
- Reference plane: die access
- V_D = +28V
- I_{DQ} = 450mA (V_G = -2.35V Typ.)
- Pin = +25dBm
- Pulsed mode (pulse width: 100µs, duty cycle: 10%)

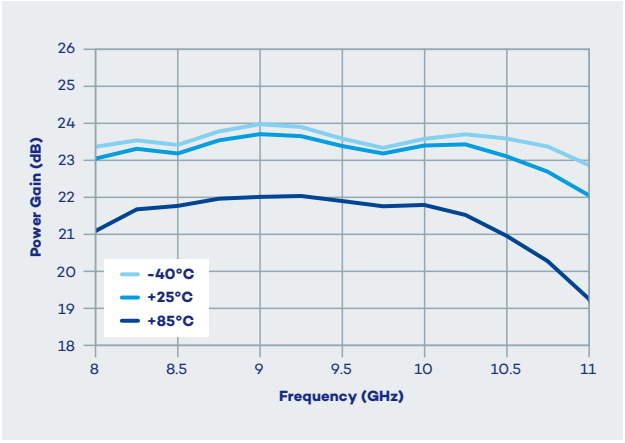
Output Power vs Frequency vs Temperature



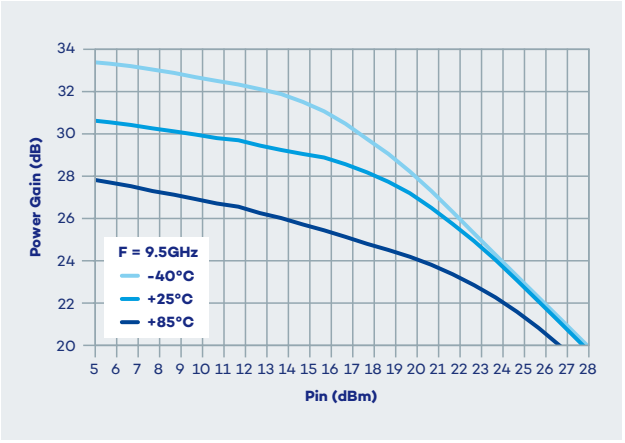
Output Power vs Input Power vs Temperature



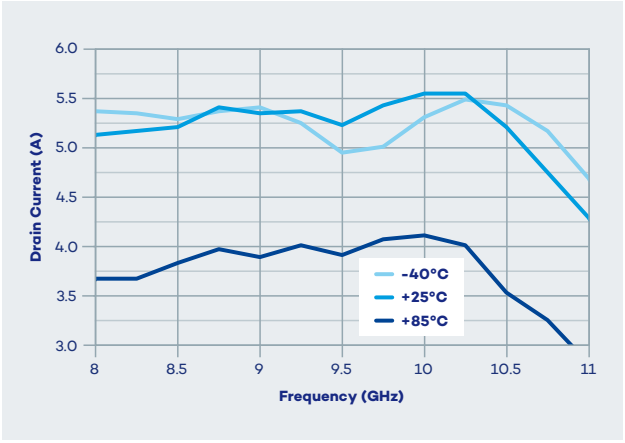
Power Gain vs Frequency vs Temperature



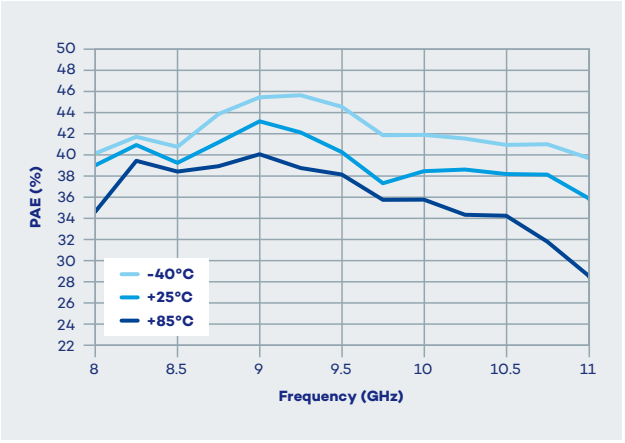
Gain vs Input Power vs Temperature



Drain Current vs Frequency vs Temperature



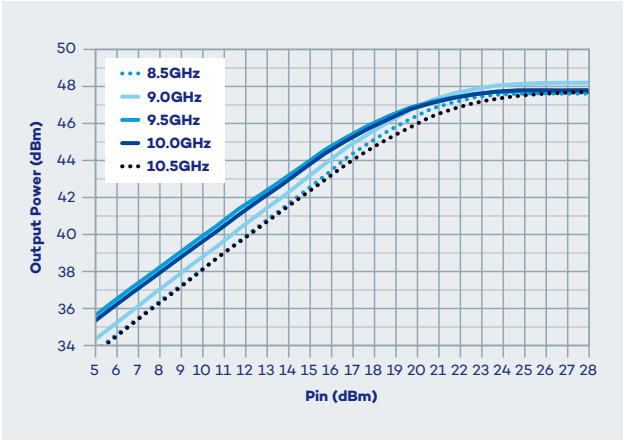
PAE vs Frequency vs Temperature



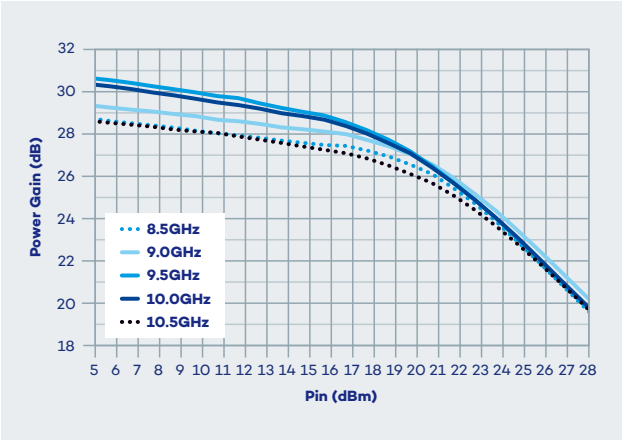
Typical Performance
(Large signal / Board Measurement)

Test conditions: unless otherwise noted
- Reference plane: die access
- V_D = +28V
- I_{DQ} = 450mA (V_G = -2.35V Typ.)
- T_{amb} = +25°C
- Pulsed mode (pulse width: 100µs, duty cycle: 10%)

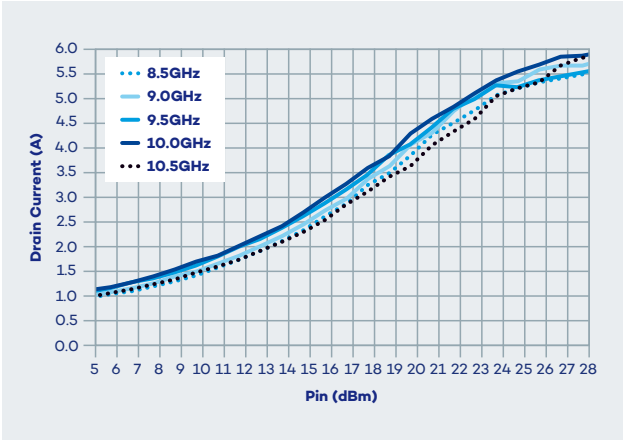
Output Power vs Input Power vs Frequency



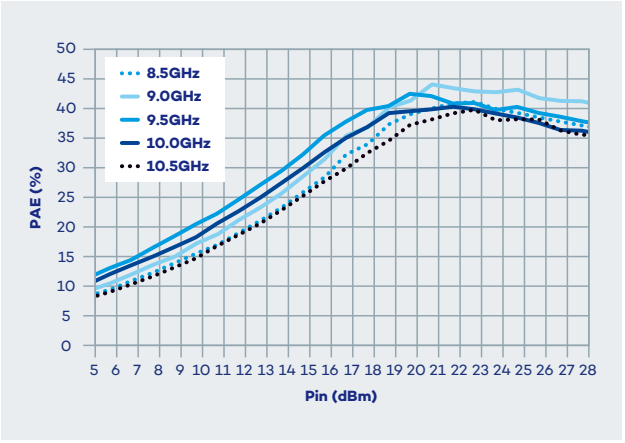
Gain vs Input Power vs Frequency



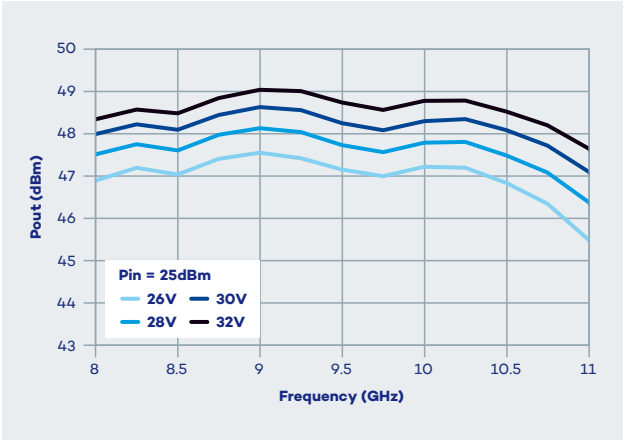
Drain Current vs Input Power vs Frequency



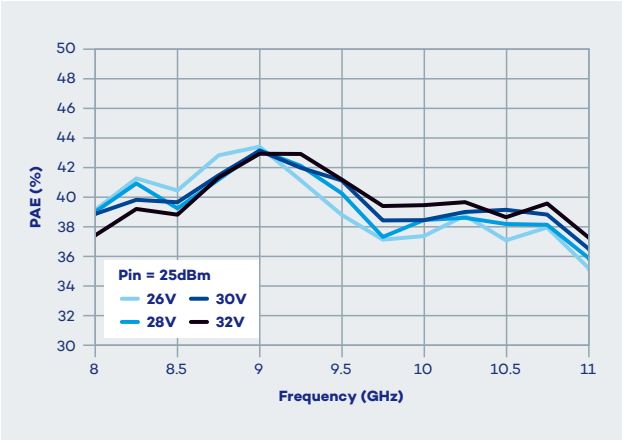
PAE vs Input Power vs Frequency



Output Power vs Frequency vs V_D



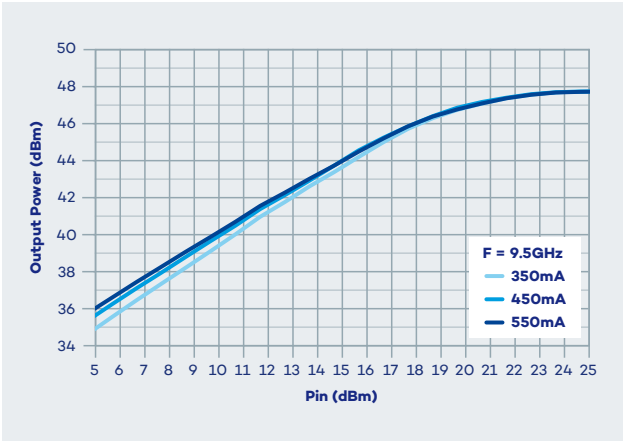
PAE vs Frequency vs V_D



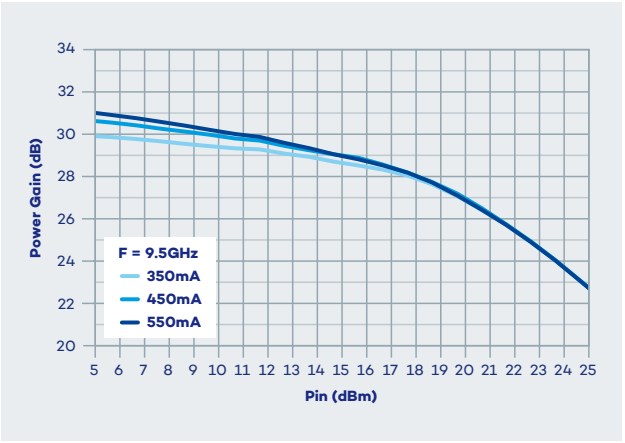
Typical Performance
(Large signal / Board Measurement)

Test conditions: unless otherwise noted
- Reference plane: die access
- V_D = +28V
- T_{amb} = +25°C
- Pulsed mode (pulse width: 100µs, duty cycle: 10%)

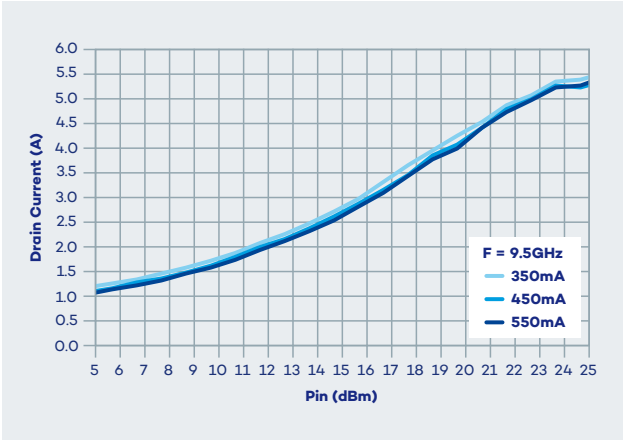
Output Power vs Input Power vs I_{DQ}



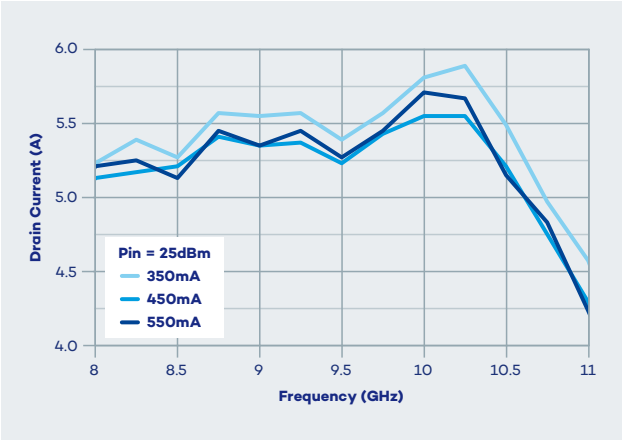
Gain vs Input Power vs I_{DQ}



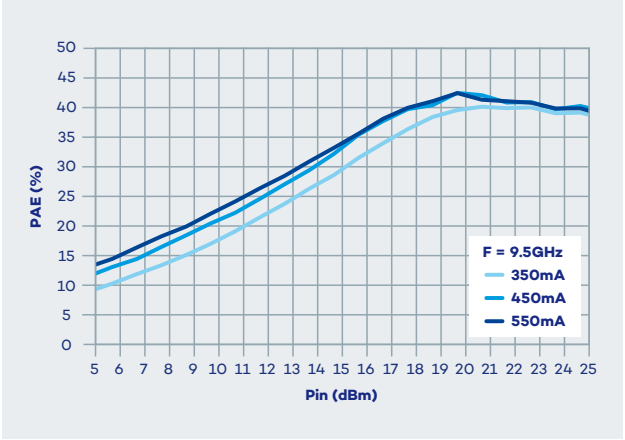
Drain Current vs Input Power vs I_{DQ}



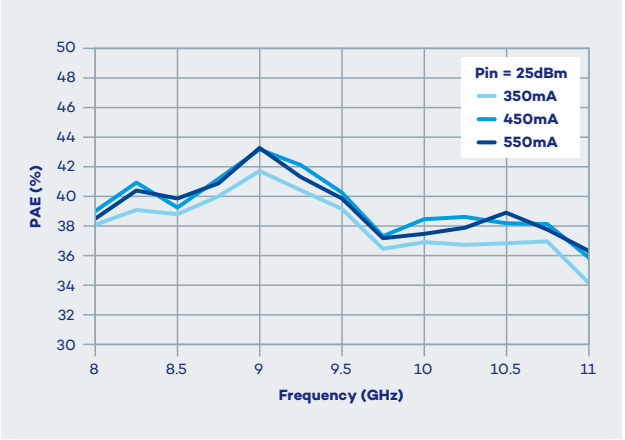
Drain Current vs Frequency vs I_{DQ}



PAE vs Input Power vs I_{DQ}



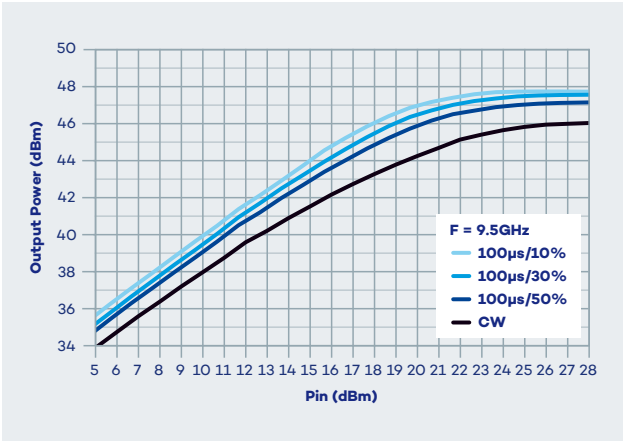
PAE vs Frequency vs I_{DQ}



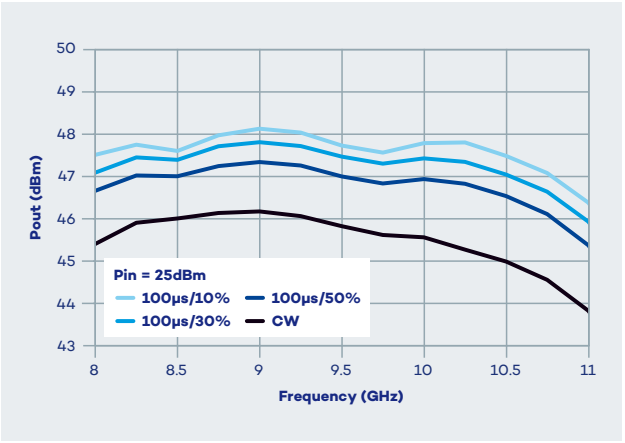
Typical Performance
(Large signal / Board Measurement)

Test conditions: unless otherwise noted
- Reference plane: component access
- V_D = +28V
- I_{DQ} = 450mA
- T_{amb} = +25°C
- Case temperature elevation of EVB: +5°C @10%, +25°C in CW mode

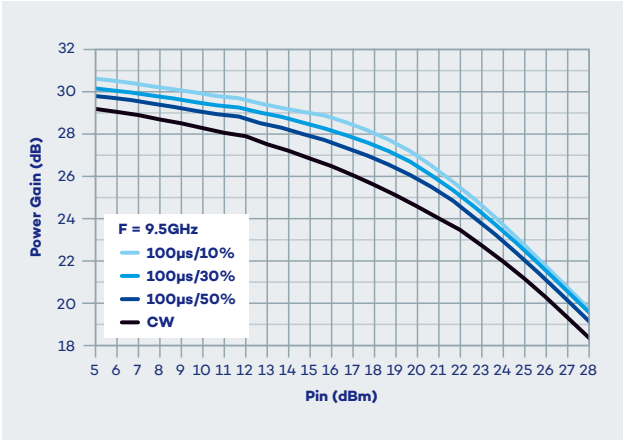
Output Power vs Input Power vs Duty Cycle



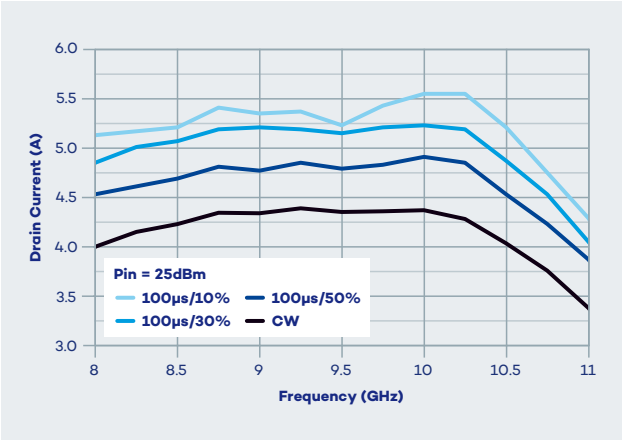
Output Power vs Frequency vs Duty Cycle



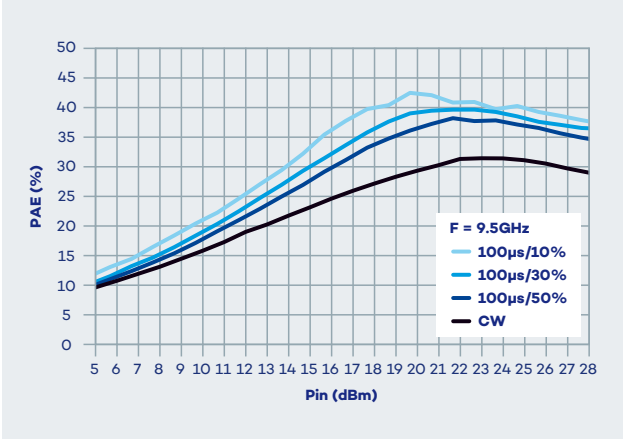
Power Gain vs Input Power vs Duty Cycle



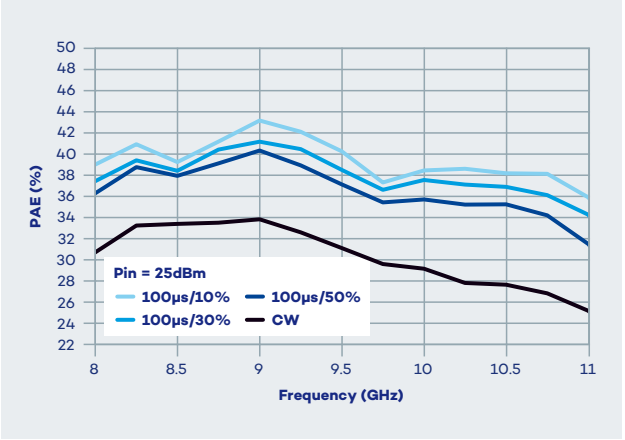
Drain Current vs Frequency vs Duty Cycle



PAE vs Input Power vs Duty Cycle

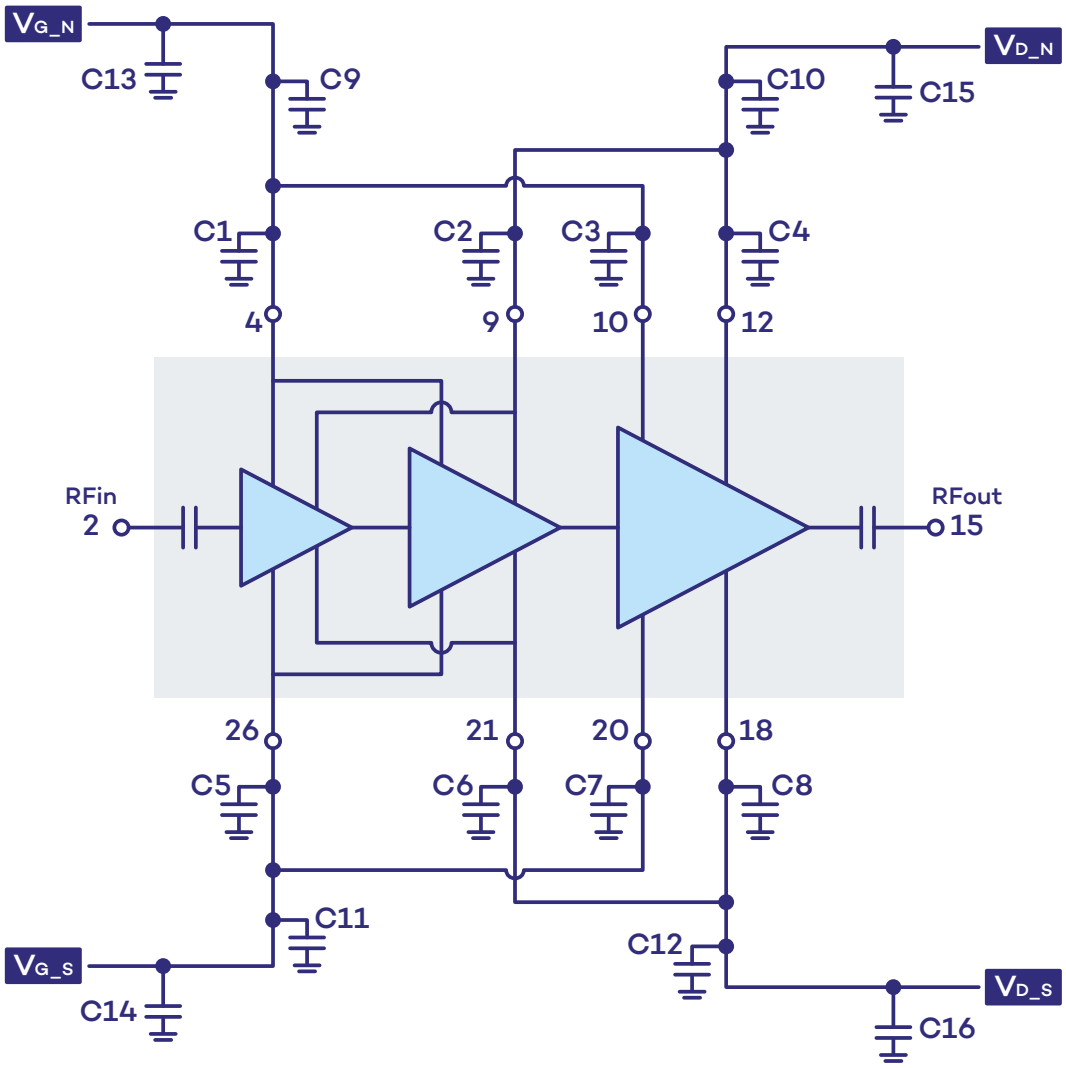


PAE vs Frequency vs Duty Cycle



Application circuit

- C1 to C8 = 1nF
- C9 to C12 = 10nF
- C13 to C16 = 1µF
- C1 to C12 should be MIM capacitors



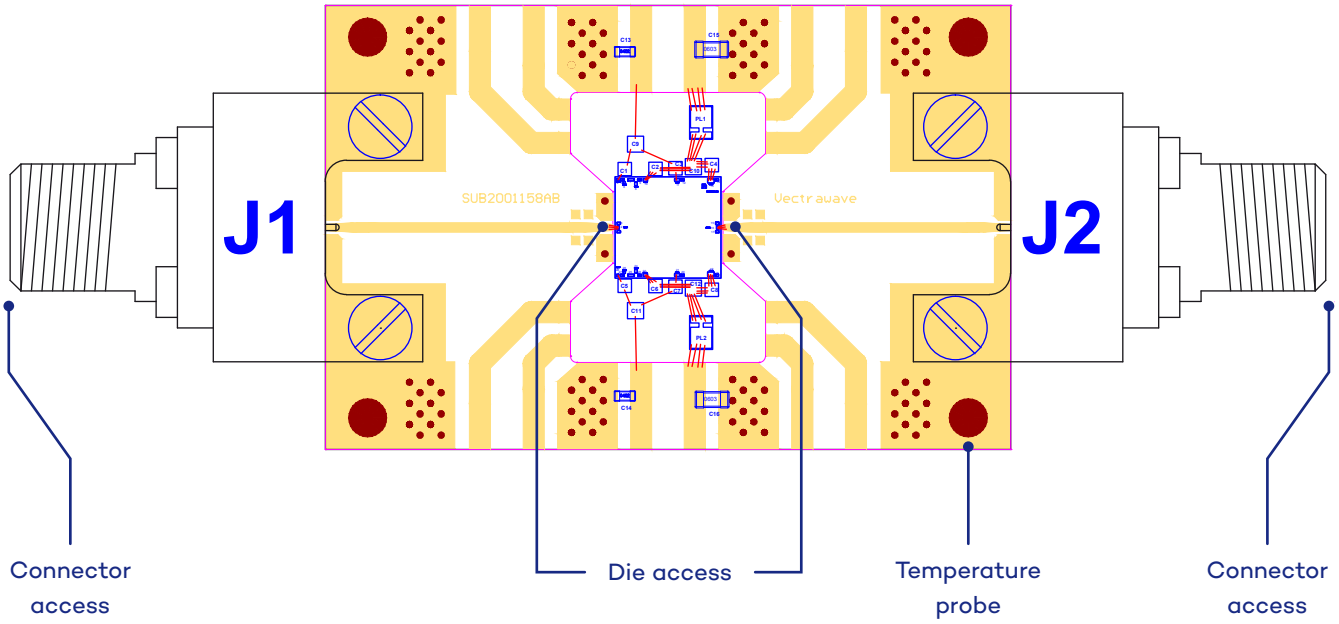
Bias-up procedure

1. Apply V_G = -3V
2. Apply V_D = +28V
3. Increase V_G to obtain the specificied I_{DQ} = 450 mA
4. Apply RF signal

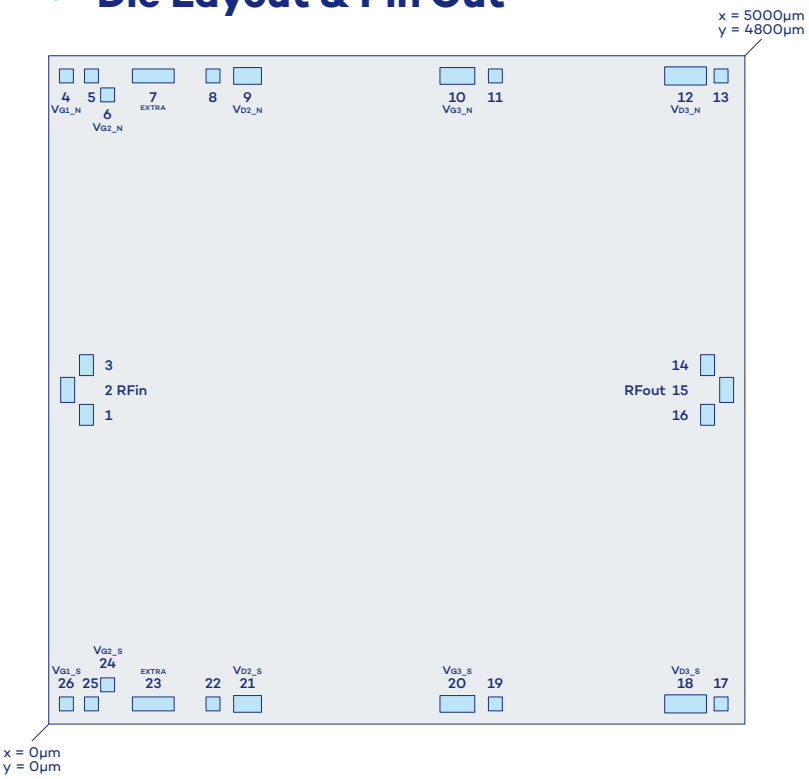
Bias-down procedure

1. Turn off RF signal
2. Reduce V_G to -3V
3. Reduce V_D to +28V
4. Turn off power supply

• Evaluation Board (EVB) Layout Assembly



Die Layout & Pin Out



- Die size = 5000µm x 4800µm
- Die thickness = 100µm
- Die size tolerance = 50µm

Pad number	Pad center X (µm)	Pad center Y (µm)	Size (µm x µm)	Name	Function
1	271	2221	100 x 150	Gnd	
2	136	2400	100 x 180	Input	RF Input
3	271	2578	100 x 150	Gnd	
4	127	4655	100 x 100	VG1_N	Gate Bias
5	307	4655	100 x 100	Gnd	
6	423	4519	100 x 100	VG2_N	Note used
7	751	4655	300 x 100	Extra	
8	1180	4655	100 x 100	Gnd	
9	1428	4655	200 x 120	VD1_N	Drain Bias
10	2935	4655	250 x 120	VG3_N	Gate Bias
11	3208	4655	100 x 100	Gnd	
12	4574	4655	300 x 130	VD3_N	Drain Bias
13	4829	4655	100 x 100	Gnd	
14	4732	2578	100 x 150	Gnd	
15	4869	2400	100 x 180	Output	RF Output
16	4732	2221	100 x 150	Gnd	
17	4829	145	100 x 100	Gnd	
18	4574	145	300 x 130	VD3_S	Drain Bias
19	3208	145	100 x 100	Gnd	
20	2935	145	250 x 120	VG3_S	Gate Bias
21	1428	145	200 x 120	VD1_S	Drain Bias
22	1180	145	100 x 100	Gnd	
23	751	145	300 x 100	Extra	
24	423	282	100 x 100	VG2_S	Note used
25	307	145	100 x 100	Gnd	
26	127	145	100 x 100	VG1_S	Gate Bias

- VG1_N & VG2_N internally connected
- VG1_S & VG2_S internally connected
- Die bottom must be connected to ground (RF and DC)
- VD1_N & VD2_N internally connected
- VD1_S & VD2_S internally connected

Ordering information

Product Code	Parameter
VM164D	8 to 10.75GHz - 50W GaN/SiC Power Amplifier in die form

Associated Material

- Packaged die
- Die Evaluation Board (die EVB)
- Packaged die Evaluation Board (packaged die EVB)
- Mechanical files (DXF)
- Measurents files (S2P)

Product Compliance Information

Solderability
Use only AuSn (80/20) solder and limit exposure to temperature above 300 °C during 3-4 minutes, maximum.

ESD Sensitivy Rating
Test: Human Body Model (HBM)
Std: JEDEC Standard JESD22-A114

RoHS-Compliance
This part is compliant with EU 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

Other attributes
- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br402) Free
- PFOS Free
- SVHC Free

Contact information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Vectrawave.

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