Vectrawave
RF & Millimeter Wave MMIC Design

DC to 44GHz - 12dB - 21dBm
Medium Power Amplifier

VM052D

General Description

The VM052D is a medium power amplifier designed on a 0.15µm pHEMT process. The device delivers more than +21dBm of output power at saturation regime, up to 40GHz, and more than +17dBm of output power at 1dB of gain compression, up to 34GHz.

It provides more than 12dB of linear gain from DC to 44GHz with a positive slope through 40GHz. This device can provide up to 11 dB gain up through 50GHz when operating with VD= 6V, with an excellent group delay.

The supply current is as low as 170mA when operated with VD= +6V.

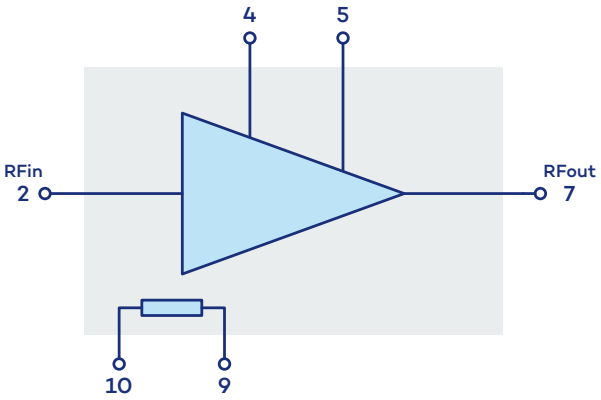
Features

Wide band	**DC – 44GHz**
Flat group delay	
50ΩRF Single ended RF input and output	
DC coupled in, DC coupled out	
P1dB	**+17dBm DC to 34GHz**
P_{SAT}	**>+21dBm DC to 40GHz**
Small signal gain	**>12dB 2GHz to 40GHz**
Power supply	**170mA @ +6V**
Chip size	**2.29 x 1.28 x 0.1 (mm)**

Applications

- Wide Band Amplifier
- Radar / ECM / ECCM
- Test and measurement
- Telecommunication format NRZ, PAM4, 56 GBPS
- Broadband / datalink communication

Pins Assignement & Functional Block Diagram



Function	Pin number
RF in	2
V_{G2}	4
V_{D_LOAD}	5
V_D & RF out	7
V_{G1_A}	9
V_{G1_B}	10

Electrical Specifications
(Test Under Probes)

Test conditions: unless otherwise noted
- T_{amb} = +25°C
- V_D = +6V
- I_D = 170mA
- V_{G2} = +2.5V

Symbol	Parameter	Min	Typ	Max	Unit
F	Frequency range	DC		40	GHz
NF	Noise figure			4	dB
G	Small signal gain		12.5		dB
ΔG	Average gain positive slope		0.0375		dB
S11	Input return loss		-10	-7	dB
S22	Output return loss		-18		dB
P1dB	Output P1dB from DC to 34GHz	17	18		dBm
P_{SAT}	Saturated output power		21		dBm
I_D	Drain current		170		mA

Environmental parameters

Symbol	Parameter	Min	Max	Unit
Top	Operating temperature range	-40	+85	°C
Tstg	Storage temperature range	-55	+85	°C

Absolute Maximum Ratings

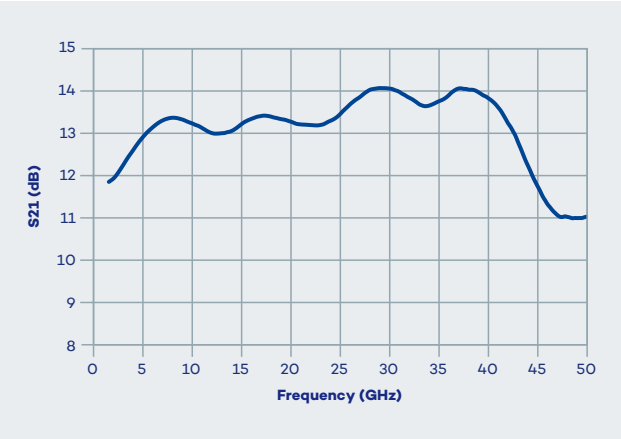
Symbol	Parameter	Min	Max	Unit
V_D	Drain bias voltage		9	V
V_{G2}	Gate control input access for second stage	-1	V_D/2	V
Pin	RF input power		18	dBm
Pdiss (CW)	Continuous power dissipation		2	W
Tprocess	Temperature process max 20 seconds		+325	°C

Operation of this device above any of these parameters may cause permanent damage.

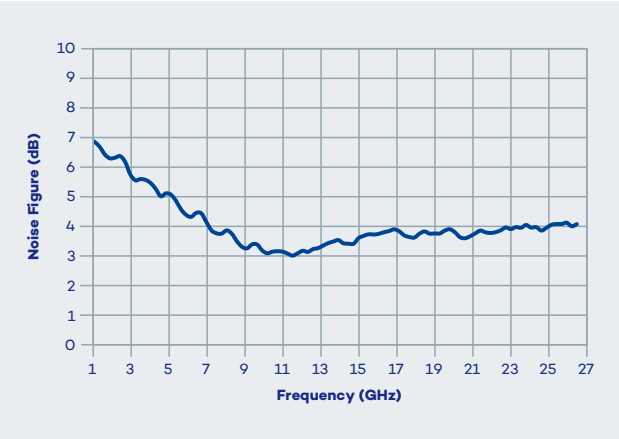
Typical Performance
(Test Under Probes)

Test conditions: unless otherwise noted
- T_{amb} = +25°C
- V_D = +6V
- I_D = 170mA
- V_{G2} = +2.5V

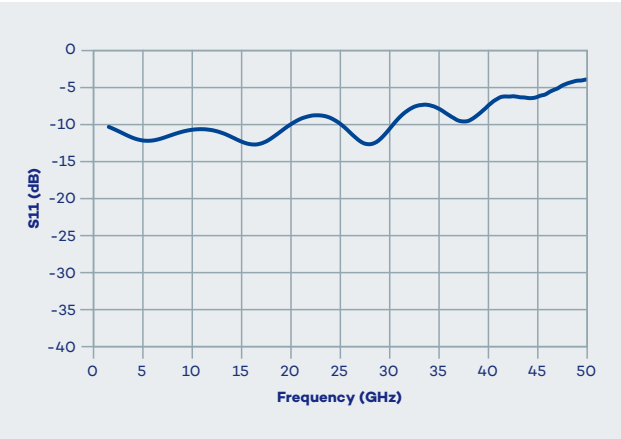
Small Signal Gain vs Frequency



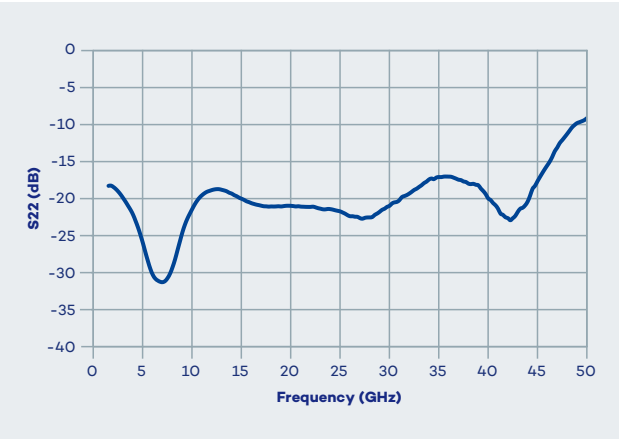
Noise Figure vs Frequency



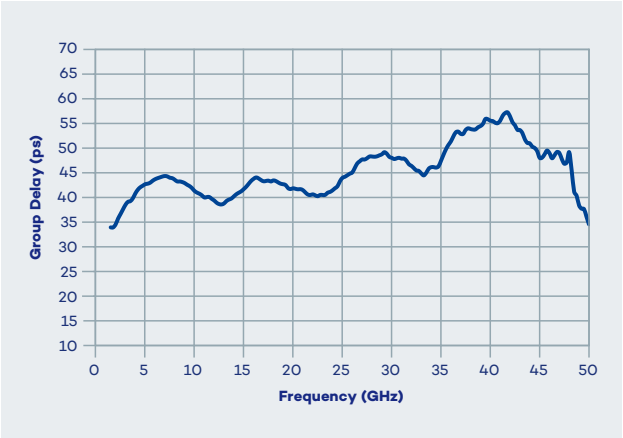
Input Return Loss vs Frequency



Output Return Loss vs Frequency



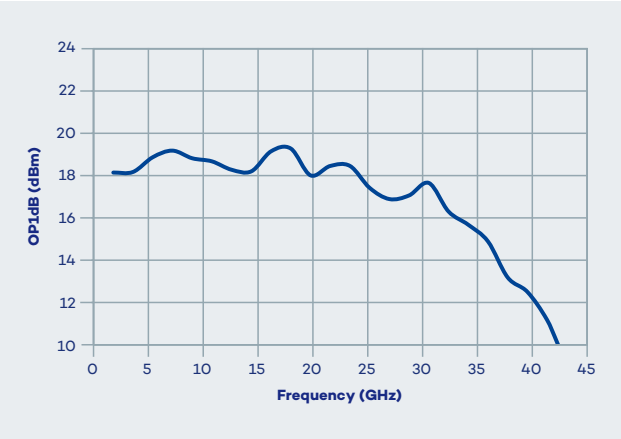
Group Delay vs Frequency



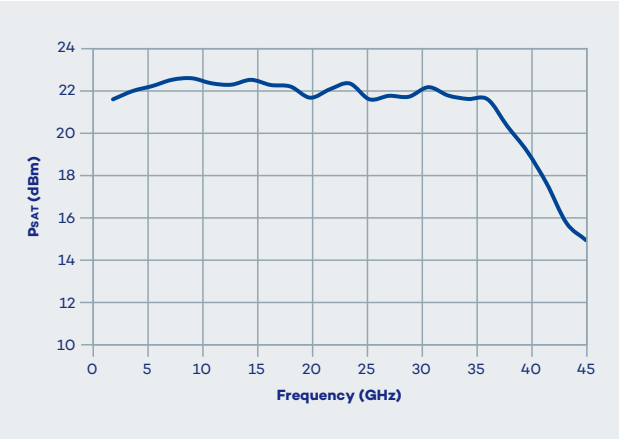
Typical Performance
(Test Under Probes)

Test conditions: unless otherwise noted
- T_{amb} = +25°C
- V_D = +6V
- I_D = 170mA
- V_{G2} = +2.5V

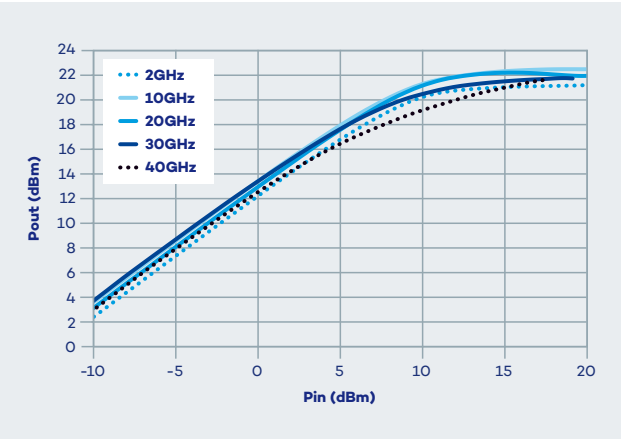
Output P1dB vs Frequency



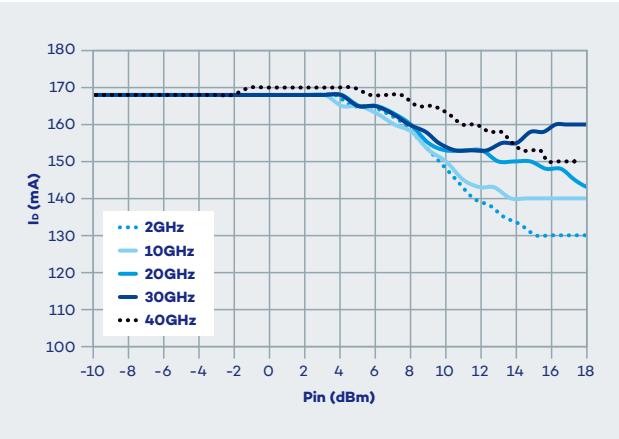
Saturated Output Power vs Frequency



Pout vs Pin vs Frequency



I_D vs Pin vs Frequency



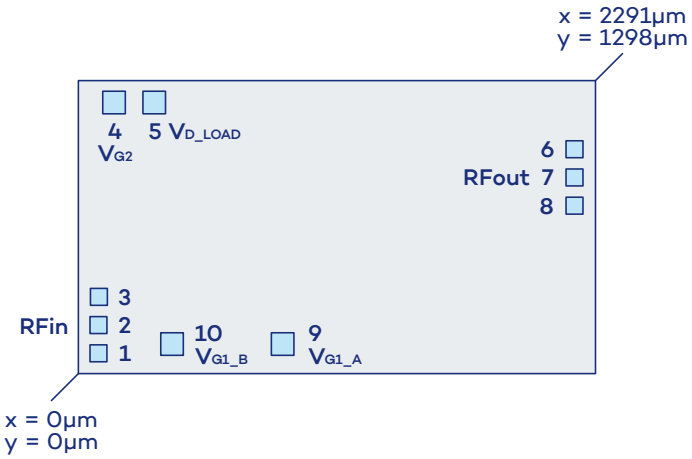
Bias-up procedure

1. Apply V_D = +6V
2. Apply V_{G2} = +2.5V
3. Apply RF signal

Bias-down procedure

1. Turn off RF signal
2. Reduce V_{G2} to 0V
3. Reduce V_D to 0V

Die Layout & Pin Out

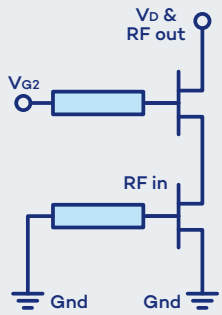
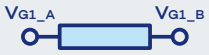


- Die size = 2291µm x 1298µm
- Die thickness = 100µm
- Die size tolerance = 50µm

Pad number	Pad center X (µm)	Pad center Y (µm)	Size (µm x µm)	Name	Function
1	89	90	75 x 75	Gnd	
2	89	215	75 x 75	RFin	RF Input
3	91	340	75 x 75	Gnd	
4	158	1201	100 x 100	V_{G2}	Gate Bias
5	336	1201	100 x 100	V_{D_LOAD}	
6	2198	994	75 x 75	Gnd	
7	2198	869	75 x 75	RFout	RF Output
8	2198	744	75 x 75	Gnd	
9	905	131	100 x 100	V_{G1_A}	Gate Bias
10	415	131	100 x 100	V_{G1_B}	Gate Bias

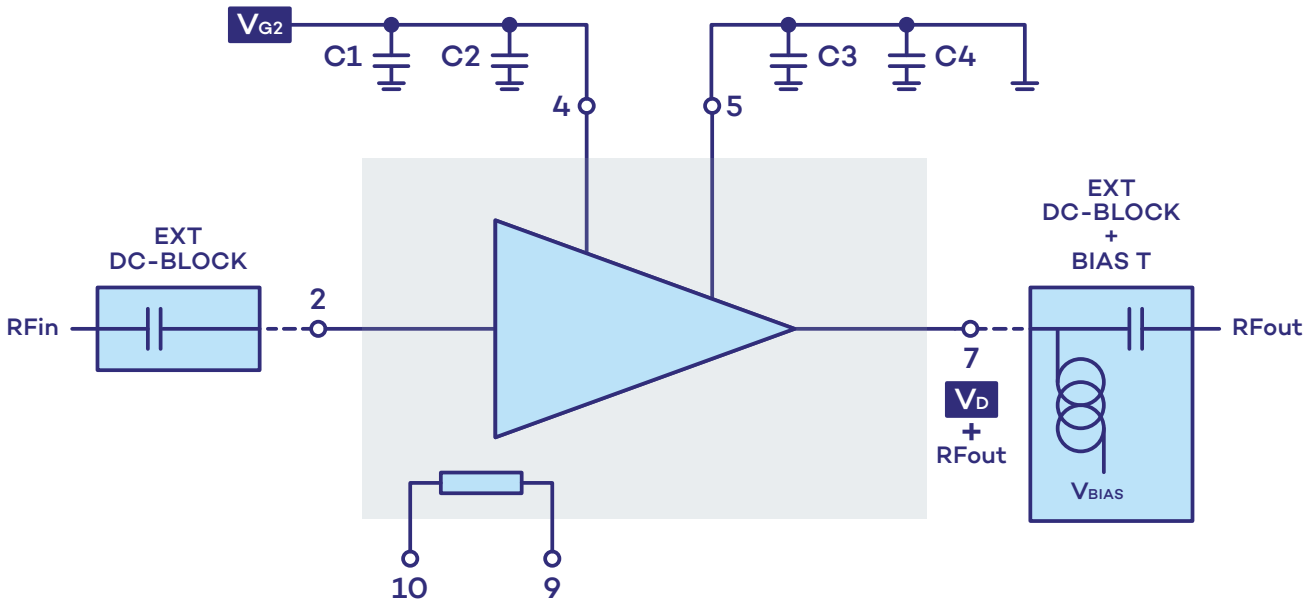
- Die bottom must be connected to ground (RF and DC)

Access description

Pin number	Name	Description	Electrical interface
2	RF in	RF Amplifier input, this access is DC coupled and internally matched to 50Ω.	
4	V_{G2}	Gate control input access for second stage distributed amplifier structure. Apply +2.5V for nominal biasing conditions.	
5	V_{D_LOAD}	Drain termination load decoupling access. For lower frequency applications, this access can be connected to a MIM 100pF or 1000pF capacitor, with a low inductance connection.	
7	RF out	RF Amplifier output, this access is DC coupled and internally matched to 50Ω. It is also used to feed the drain current (I_D), by using a wide bandwidth external Bias-T structure.	
9	V_{G1_A}	Gate control input access for first stage distributed amplifier structure. Unused for nominal biasing conditions.	
10	V_{G1_B}	Gate control output access for first stage distributed amplifier structure. Unused for nominal biasing conditions.	
Die Bottom	Gnd	Die must be connected to RF and DC Ground	

Application circuit

- C1 and C4 = 1µF
- C2 and C3 = 1nF capacitors are MIM type and must be placed as close as possible to the die access.



Ordering information

Product Code	Parameter
VM052D	DC to 44GHz - 12dB - 21dBm Medium Power Amplifier

Associated Material

- Packaged die
- Die Evaluation Board (die EVB)
- Packaged die Evaluation Board (packaged die EVB)
- Mechanical files (DXF)
- Measurents files (S2P)

Product Compliance Information

Solderability
Use only AuSn (80/20) solder and limit exposure to temperature above 300 °C during 3-4 minutes, maximum.

ESD Sensitivy Rating
Test: Human Body Model (HBM)
Std: JEDEC Standard JESD22-A114

RoHS-Compliance
This part is compliant with EU 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

Other attributes
- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C15H12Br402) Free
- PFOS Free
- SVHC Free

Contact information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about Vectrawave.

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